Electrical properties of hafnium silicate gate dielectrics deposited directly on silicon

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Hafnium silicate ($HfSi_xO_y$) gate dielectric films with ~6 at.% Hf exhibit significantly improved leakage properties over SiO_2 in the ultrathin regime while remaining thermally stable in *direct contact* with Si. Capacitance–voltage measurements show an equivalent oxide thickness (t_{ox}) of less than 18 Å for a 50 Å $HfSi_xO_y$ film deposited directly on a Si substrate, with no significant dispersion of the capacitance for frequencies ranging from 10 kHz to 1 MHz. Current–voltage measurements show for the same film a leakage current of 1.2×10^{-6} A/cm^2 at 1 V bias. Hysteresis in these films is measured to be less than 20 mV, the breakdown field is measured to be E_{BD} ~10 MV/cm, and the midgap interface state density is $D_{it}\sim10^{11}\,cm^{-2}\,eV^{-1}$. Cross-sectional transmission electron microscopy shows no signs of reaction or crystallization in $HfSi_xO_y$ films on Si after being annealed at 800 °C for 30 min. © *1999 American Institute of Physics.* [S0003-6951(99)03917-0]

Replacing silicon dioxide as the gate dielectric material for standard complementary metal oxide semiconductor (CMOS) technology is a formidable task, considering that SiO_2 has been used successfully for decades and its properties are understood at least as well as those of any dielectric. The area of advanced gate dielectrics has gained considerable attention recently, however, because technology roadmaps predict the need for a sub-20 Å oxide for a sub-0.1 μm CMOS, and there are significant leakage current and reliability concerns for SiO_2 in this thickness regime.[1] Efforts are being focused on altering the gate stack, rather than just the gate dielectric, because most of the high dielectric constant (high-ϵ) materials currently being studied, including Ta_2O_5,[2–5] TiO_2,[6] $SrTiO_3$,[7] and Al_2O_3,[8] have ϵ values ranging from 10 to 80, but are not thermally stable in direct contact with Si (Al_2O_3 is a possible exception). In particular, interfacial reaction has been observed for the case of Ta_2O_5 on Si.[9]

In an attempt to prevent or at least minimize reaction with the underlying Si, interface engineering schemes have been developed to form oxynitrides and oxide/nitride reaction barriers[2–6] between the high-ϵ material and Si. While these barrier layers have been shown to reduce the extent of reaction between the high-ϵ dielectric and Si, the increased process complexity for the deposition and control of additional ultrathin dielectric layers, as well as scalability to later technology nodes, is a large concern. Even in the ideal case of completely eliminating interfacial reaction, the structure still contains several dielectrics in series, where the lowest capacitance layer will dominate the overall capacitance and also set a limit on the minimum achievable equivalent oxide thickness (t_{ox}) value. Each additional interface between dielectrics also serves as a potential source of electron traps and charging.

Metal gates such as TiN have been used with most of the high-ϵ dielectrics mentioned above to prevent reaction at the gate interface. Although metal gates are desirable for eliminating dopant depletion effects, for the case of sub-0.1 μm bulk CMOS devices, the high threshold voltage created by midgap work function (Φ_B) metals (e.g., TiN) has been predicted not to provide a performance improvement worthy of the added process complexity to replace Si-based gates.[10]

In order to obtain low leakage currents, it is important to find a gate dielectric which remains amorphous during post-processing treatments, since grain boundaries may serve as high leakage paths. It is therefore desirable to employ a dielectric which exhibits an enhanced permittivity over that of SiO_2, remains amorphous during processing, and avoids the need for a reaction barrier at the interface.

An important approach toward understanding and predicting the relative stability of a particular three-component system for device applications can be explained through thermodynamic arguments and ternary phase diagrams.[11–13] An analysis of the Gibbs free energies governing the relevant chemical reactions for the Ta–Si–O and Ti–Si–O ternary systems, for example, indicates that Ta_2O_5 and TiO_2 (or mixtures with Si), respectively, are not stable to SiO_2 formation when placed next to Si,[11] and this is observed experimentally.[9,14] On the other hand, the phase diagram for the Zr–Si–O system,[15] which is expected to be the same for the Hf–Si–O system based on coordination chemistry, predicts that the metal oxide ZrO_2 as well as the compound silicate $ZrSiO_4$ will be stable in direct contact with Si. Although there is incomplete thermodynamic information on the Hf–Si–O system, the available data[16–18] suggest that HfO_2 and $HfSi_xO_y$ will be stable in direct contact with Si up to high temperatures.

Based on the desirable properties for a gate dielectric material mentioned above, hafnium silicate ($HfSi_xO_y$) is a promising material. HfO_2 and ZrO_2 exhibit high-ϵ values, and are nominally stable on Si, but both oxides crystallize at relatively low temperature, and it is likely that Si will diffuse into the oxide film, forming an uncontrolled, poor-quality

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silicate layer. Depositing a controlled silicate layer from the onset should provide superior properties. There has been much less information reported on $HfSi_xO_y$ than on zirconium silicate ($ZrSi_xO_y$), but the chemical similarities between Hf and Zr allow for comparison between the respective silicate systems. As described by Blumenthal,[19] the crystal structure for the stoichiometric compound $ZrSiO_4$ is tetragonal, and is composed of parallel chains of –Zr–2O–Si–2O–Zr–2O–Si–,..., where each Zr and Si atom shares bonds to four O atoms within the chain. In addition, each Zr and Si atom also shares two other O atoms with neighboring chains, providing a three-dimensional stability to the material. The structural units are ZrO_2 and SiO_2 molecules. Analogously, $HfSiO_4$ should have the same structure. A value of $\epsilon=12.6$ for $ZrSiO_4$ is reported by Blumenthal,[19] which is reasonable considering that this structure is comprised of SiO_2 ($\epsilon=3.9$) and ZrO_2 ($\epsilon=25$) components. Similarly, since HfO_2 has $\epsilon=40$, a $HfSiO_4$ compound is expected to have a dielectric constant in the range of $\epsilon=15-25$. The exact value of ϵ will certainly depend strongly on film composition density and structure, since amorphous materials, which are used in this study, typically have less lattice polarizability than their crystalline counterparts. Considering all of the desired properties these materials possess, both $HfSi_xO_y$ and $ZrSi_xO_y$ (Ref. 20) should be excellent materials candidates for advanced gate dielectrics. In this letter, it is shown that a thin dielectric layer of $HfSi_xO_y$ with ~6 at. % Hf yields $t_{ox}<18$ Å with a leakage current density of $\sim 1\times10^{-6}$ A/cm^2, while remaining amorphous and stable in direct contact with Si.

Substrates were 4 in., *n*-type Si(100) wafers, with $\rho=0.01-0.02\,\Omega$ cm. Samples were prepared by etching in a buffered (1%) HF solution for 20 s, leaving an H-terminated surface. Once under vacuum, hydrogen was desorbed by annealing the wafer at 700 °C for 10 min. $HfSi_xO_y$ films were sputter deposited in a system with a base pressure of 5×10^{-9} Torr, with sputter rates of 5–6 Å/min and substrate temperatures ranging from 25 to 600 °C. The substrates were heated radiatively from the backside, with an absolute temperature accuracy of ±20 °C over the temperature range used. X-ray photoelectron spectroscopy (XPS) and Rutherford backscattering spectrometry (RBS) measurements showed the film composition to be approximately $Hf_6Si_{29}O_{65}$ (±1 at. % for Hf). The Hf content was limited by source target composition and deposition conditions. Peaks for Si–O and Hf–O bonds were visible in the XPS spectra, but the Hf–O peaks were shifted higher in energy than the reference. Hf–O peaks in a pure HfO_2 film. This distinguishes Hf–O bonds for silicates, which are in the vicinity of Si atoms, from those in pure HfO_2. Peaks for Hf–Si bonds were not detected. This indicates that a silicate was indeed formed, as opposed to a phase-separated system.

Capacitors were formed using Au *ex situ* thermal evaporation, followed by photolithography and wet etching steps to pattern the electrodes (Al electrodes were also fabricated, and were seen to react with the silicates[20]). Capacitance–voltage ($C-V$) measurements were performed on a HP 4284 *LCR* meter at frequencies up to 1 MHz. Capacitor areas ranged from 10^{-6} to 10^{-2} cm^2, and both capacitance and current scaled linearly with area, indicating uniform, high-quality films.

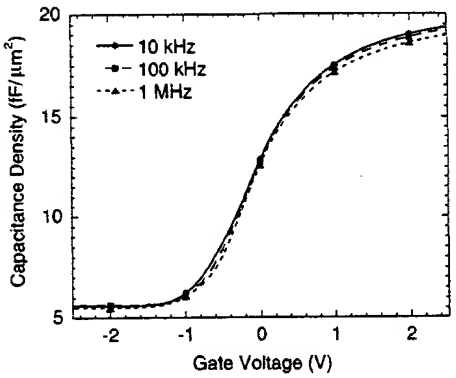

FIG. 1. $C-V$ curves of a 50 Å $HfSi_xO_y$ film, deposited at 500 °C and subsequently annealed in forming gas at 450 °C for 30 min., with Au electrodes ($A=1.76\times10^{-4}$ cm^2). The capacitance density in accumulation yields $t_{ox}=17.8$ Å. These films have $V_{fb}\sim0$ V, but the slight dispersion near zero bias indicates the presence of some interface traps.

The $C-V$ characteristics of a Au/50 Å $HfSi_xO_y/n^+$Si structure are shown in Fig. 1, with an electrode area of 1.76×10^{-4} cm^2. The $HfSi_xO_y$ film was deposited directly on Si at 500 °C and postannealed in forming gas (90% N_2:10% H_2) at 450 °C for 30 min. The largest value of measured capacitance density in accumulation is $C_{max}/A=19.3$ fF/μm^2, which corresponds to $\epsilon\sim11$, or an equivalent oxide thickness of $t_{ox}=17.8$ Å, where t_{ox} is the electrical thickness equivalent for pure SiO_2.[21] To our knowledge, this is the first reported oxide equivalent below 20 Å for a single-layer advanced gate dielectric deposited directly on Si.

Figure 1 also demonstrates that the Au electrode, with a work function $\Phi_B=5.3$ eV, creates a flatband condition at zero bias ($V_{fb}\sim0$ V). Au was chosen for its chemical inertness and because of its relatively large Φ_B, to create $V_{fb}\sim0$ V for this system. Work is underway to measure devices with doped poly-Si electrodes. There is a slight frequency dependence of the capacitance between 10 kHz and 1 MHz near zero bias, indicating that there are interface traps which cannot respond at high frequency. Although no experiments were done to directly measure midgap interface state density (D_{it}), comparison of the 100 kHz curve to an ideal $C-V$ curve indicates that $D_{it}\sim10^{11}$ cm^{-2}eV^{-1}. The 100 kHz curve is an overlay of both positive and negative $C-V$ sweeps, which shows a hysteresis of less than 20 mV. Since silicates have SiO_2 molecular units, and have similar Si–O bond lengths (1.62 Å) to pure SiO_2, it is not surprising that forming gas sinters work well for these materials.

Figure 2 displays the $I-V$ characteristics for the film shown in Fig. 1, with the same Au electrode area. The leakage current density is very low for this film, ranging from 10^{-6} to 10^{-5} A/cm^2 in the bias range from 1.0 to 1.5 V. A pure SiO_2 layer of the same electrical ~18 Å thickness[22] has a current density of approximately 1 A/cm^2, nearly six orders of magnitude higher leakage current than that for an electrically equivalent $HfSi_xO_y$ film. For devices that were ramped to hard breakdown, the breakdown field (E_{BD}) was consistently measured to be $E_{BD}\sim10$ MV/cm. The $I-V$ curve is also seen to be nearly symmetrical, indicating that transport under both gate and substrate injection is limited by the same

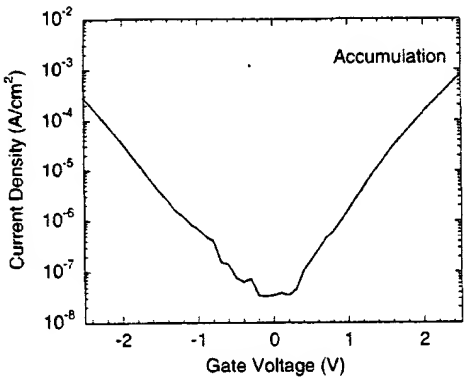

FIG. 2. Corresponding $I-V$ curve for the sample illustrated in Fig. 1. The film shows a low leakage current density of 1.5×10^{-6} A/cm^2 at 1 V bias, and the $I-V$ curve is well behaved. The symmetry indicates nearly the same barrier in both polarities.

activation energy, which most likely corresponds to the same barrier height at both $HfSi_xO_y$ interfaces. The noisy portion of the $I-V$ curve between -0.8 and $+0.8$ V is attributed to very small absolute currents, in the 1–10 pA range. The overall greatly reduced leakage currents measured for $HfSi_xO_y$ result from the physically thicker 50 Å film as well as from the amorphous structure of the film.

Figure 3 shows high-resolution transmission electron microscope (TEM) images of a 50 Å $HfSi_xO_y$ film before and after annealing. Figure 3(a) shows the as-deposited film, which was deposited at a substrate temperature of 500 °C, with a Au cap. The $HfSi_xO_y$–Si interface is seen to be atomically sharp, and the silicate is completely amorphous. Figure 3(b) shows the same film after an anneal at 800 °C for 30 min in a N_2 ambient (Au deposited after anneal). The interface remains sharp and the thickness of the layer shows no visible change after anneal at high temperature, which demonstrates the stability of the $HfSi_xO_y$ films in direct contact with Si. Au lattice fringes are visible in areas of both (a) and (b).

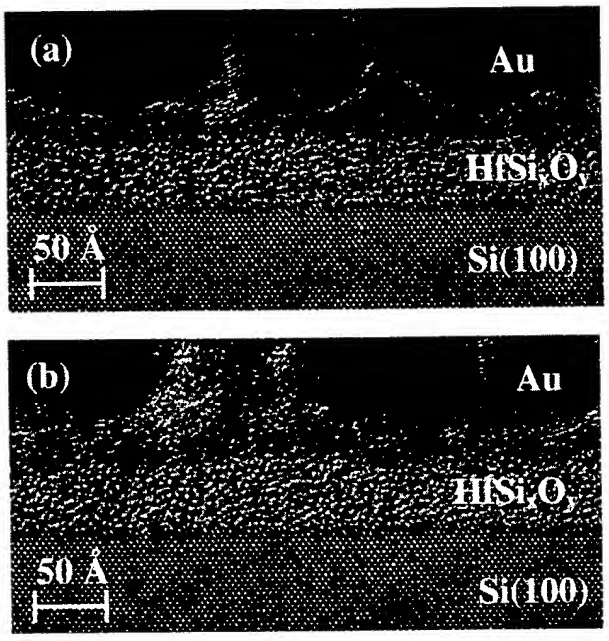

FIG. 3. High-resolution TEM images of a 50 Å $HfSi_xO_y$ film with a Au cap. (a) as deposited at 500 °C, the film is uniform and has an atomically flat interface with Si; (b) after anneal in N_2 at 800 °C for 30 min, the film shows no visible reaction. and a sharp interface with Si is maintained.

Since these films were limited to low Hf levels by the source target composition and deposition conditions, $HfSi_xO_y$ films which have compositions closer to stoichiometric $HfSiO_4$ are expected to exhibit a further increased ϵ value. Obtaining the $HfSiO_4$ stoichiometry should not be necessary, however, especially since it is desirable to maintain an amorphous structure. Any film composition which is somewhat Si rich will be suitable, to help prevent the formation of crystalline HfO_2 precipitates and associated structural and electrical defects during any postprocessing steps.

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[21] Based on $C=\epsilon\epsilon_0 A/t$ for a parallel-plate capacitor, where ϵ = relative dielectric constant, $\epsilon_0=8.85\times10^{-14}$ F/cm, A = capacitor area, and t = electrical dielectric thickness. Thus, $t_{ox}=3.9\epsilon_0(A/C_{max})$, and C/A = 34.5 fF/μm^2 corresponds to $t_{ox}=10$ Å.
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Ultrathin zirconium silicate film with good thermal stability for alternative gate dielectric application

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Zirconium silicate ($ZrSi_xO_y$) films have been sputtered by comagnetron-reactive sputtering. The composition of $ZrSi_xO_y$ has been controlled by adjusting the sputtering powers of Si and Zr targets to achieve various effective dielectric constants. The sputtered silicate layers showed low equivalent oxide thickness of 14.5 Å with a low leakage of 3.3×10^{-3} A/cm^2 at -1.5 V relative to flat band voltage. The silicate films also exhibited good high-temperature stability and smooth interfacial properties on silicon substrate. © *2000 American Institute of Physics.* [S0003-6951(00)01337-1]

Various kinds of high-k materials have been studied to replace conventional thermal oxide or oxynitride. Due to their thermodynamic stability in contact with silicon, ZrO_2, HfO_2, and their silicates have attracted a lot of attention recently.[1–5] They can be deposited directly on Si without any barrier layers. Transmission electron microscopy (TEM) images also revealed that for ZrO_2 and HfO_2 films, there is an interfacial layer between the high k and Si substrate.[1] The interfacial layer is probably formed due to the excess oxygen in the deposition chamber or the annealing furnace. This interfacial layer has been identified as a silicate layer with a higher dielectric constant than SiO_2.[1] In fact, this silicate layer is important to reduce the interface state density and it remains amorphous even after high-temperature annealing (>1000 °C). Experimental results show that for both ZrO_2 and HfO_2, the equivalent oxide thickness increases with thermal annealing.[1,2] This is due to the interfacial silicate layer growth. Russak *et al.*[6] reported that even a small amount of SiO_2 (10 at. %) can stabilize the mixed film of ZrO_2 and SiO_2 in an amorphous phase. Furthermore, the bonding in ZrO_2 is ionic, the oxygen ion diffusivity is high whereas in Zr silicate the oxygen atoms are covalently bonded and hence do not have high ion diffusivity.

Hf and Zr silicates have been fabricated by sputtering from silicate targets.[3–5] However, the range of Hf and Zr composition can be limited by the target composition, nevertheless, good capacitance equivalent oxide thickness values of about 18 Å for Hf silicate, and 21 Å for Zr silicate were reported.[3–5] TEM images showed a single layer of an amorphous silicate structure. It was pointed out that the silicate layer should be Si rich to avoid precipitation of nucleated Hf or Zr oxide and to maintain an amorphous structure. Furthermore, since these silicate layers are Si rich, they may have a better compatibility with conventional polysilicon process. In this letter, we will present the Zr silicates prepared by comagnetron-reactive sputtering; different compositions of $ZrSi_xO_y$ with dielectric constants from 7.5 to 12.4 have been obtained. These films show low leakage and high thermal stability up to 900 °C without causing an increase of the equivalent oxide thickness.

p-Si(100) wafers with a resistivity of 5–25 Ω cm were used as substrates. Field oxide of about 3500–4000 Å were grown, patterned, and etched to form the active area. Before Zr silicate deposition, the wafers were piranha cleaned and dipped in HF solution (1:40). The sputtering system has a base vacuum of about 2×10^{-7} Torr. Zr (99.7% pure) and undoped Si were used as the targets. The sputtering pressure was 40 mTorr ($Ar+O_2$) with an O_2 flow rate of 2 sccm. The wafer temperature was 500 °C, the Si sputtering power was 100 W, and the Zr sputtering power varied from 200 to 500 W. The substrate to target distance was about 10 cm for the Si target, and 30 cm for the Zr target, respectively. The film thickness was measured using the ellipsometry technique. After the silicate sputtering, the films were rapid thermal annealed in N_2 ambient at temperatures from 600 to 1000 °C. Pt was sputtered and patterned as the gate electrode followed by etching using aqua regia solution ($HCl:H_2O:HNO_3=7:5:1$) at 75 °C. Al was evaporated on the back side of the wafers to ensure a low contact resistance. The Zr silicate composition was measured by Rutherford backscattering spectroscopy (RBS). Capacitance–voltage ($C-V$), current–voltage, and hysteresis were measured using Hewlett Packard 4156 and 4194 parameter analyzers. The equivalent oxide thickness was calculated from the accumulation capacitance of the $C-V$ curve with the consideration of quantum mechanical effects.[7]

Figure 1 shows the Zr concentration (measured by RBS) and the corresponding effective dielectric constant of these silicate films after an 800 °C, 30 s, N_2 anneal. The Zr concentration was measured using RBS from thicker films (>300 Å). The effective dielectric constant was calculated from the physical thickness and the equivalent oxide thickness. The physical thickness of Zr silicates is in the range of 40–60 Å measured by ellipsometer. For some samples, the physical thicknesses were confirmed by TEM. By varying the Zr sputtering power, various Zr concentrations in silicate films can be obtained. Meanwhile, the Zr concentration was kept below the maximum concentration in stoichiometric $ZrSiO_4$ to prevent ZrO_2 precipitation. It can be clearly seen that the effective dielectric constant increases proportionally as the Zr concentration was increased. For 15% Zr silicate,

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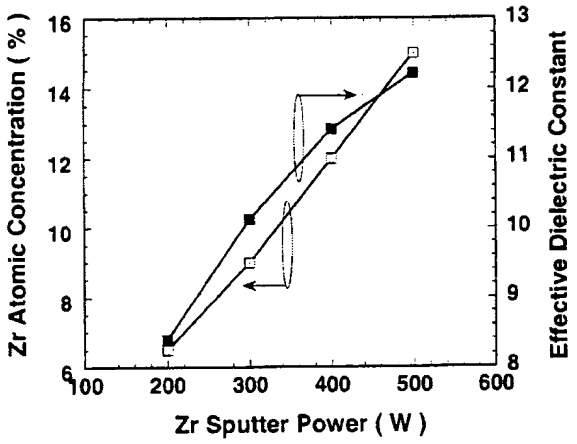

FIG. 1. Zr concentration and effective dielectric constant of Zr silicate as a function of the Zr sputtering power. The silicon sputtering power was fixed at 100 W.

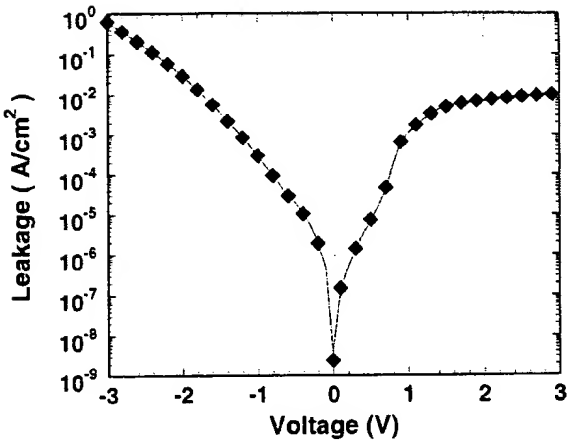

FIG. 3. Leakage current of the 14.5 Å equivalent oxide thickness Zr silicate (12% Zr) gate dielectric. Zr silicate exhibit low leakage of 3.3 $\times 10^{-3}$ A/cm^2 at -1.5 V relative to flat band voltage. The area of the capacitors is 5×10^{-5} cm^2.

the dielectric constant obtained was close to the ideal value for $ZrSiO_4$ of around 12.7[8].

Figure 2 shows the $C-V$ curves for 12.0% Zr silicate films after a 700 °C, 10 s, N_2 anneal. The capacitor area is 5×10^{-5} cm^2. Well-behaved $C-V$ curves were obtained with an equivalent oxide thickness of 14.5 Å. Also shown is the simulated low frequency $C-V$ curve of the 14.5 Å equivalent oxide thickness Zr silicate. It can be seen that the experimental and simulated $C-V$ curves fit quite well. The hysteresis is also shown in Fig. 2. The positive and negative sweep $C-V$ curves are almost the same, indicating a negligible $C-V$ hysteresis (less than 10 mV). By using the Terman method, the interface state density can be estimated, which gives the value of less than 10^{11} cm^{-2} eV^{-1}.

The leakage current was measured with the lights on to enhance the minority carrier generation. The area of the capacitor is 5×10^{-5} cm^2. Figure 3 illustrates the leakage of Pt/Zr silicate (12.0% Zr)/p-Si. The flatband voltage from the $C-V$ shown in Fig. 2 is about 0 V, the leakage current at -1.5 V($V_g-V_{fb}=-1.5$ V) is about 3.3×10^{-3} A/cm^2. Although direct comparison with SiO_2 is difficult due to different electrode materials (Pt vs poly), this leakage is orders of magnitude lower than SiO_2 ever reported.[9]

Figure 4 is a high resolution TEM image of Zr silicate (12% Zr) on Si substrate after an 800 °C, 30 s, N_2 rapid thermal anneal. As expected, amorphous structure can be observed with good uniformity. No ZrO_2 precipitates were formed, even after 800 °C annealing. This result is in agreement with previous reports.[3,6] This amorphous structure may be helpful to achieve low leakage current. Another observation is that there is no interfacial layer between silicate and Si substrate, and the interface between silicate and Si is sharp. Similar results were reported by Wilk *et al.* for the silicate films sputtered from the silicate targets.[3–5] The good interface between silicate and Si is due to the small amount of Zr in the silicate and the good thermal stability of the silicate film. $C-V$ measurement also showed that even after a 900 °C anneal, the equivalent oxide thickness of silicate remains the same (data not shown). When annealing at temperatures higher than 900 °C, a slight equivalent oxide thickness increase (~4 Å) was observed. TEM does not show crystallization or precipitates. Our data from another experiment show that ZrO_2 is compatible with polysilicon gate electrode (data not shown). Work is being done to investi-

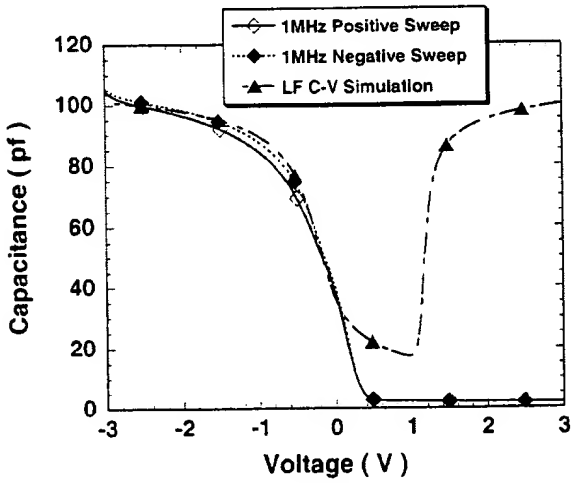

FIG. 2. High frequency $C-V$ curves of Pt/Zr–silicate/Si, minimum hysteresis of less than 10 mV was obtained. Also shown is the simulated low frequency $C-V$ curve, taking the quantum mechanical effects into consideration, an equivalent oxide thickness of 14.5 Å was obtained. The capacitor area is 5×10^{-5} cm^2.

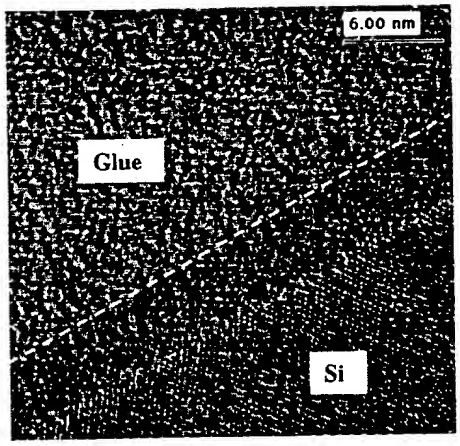

FIG. 4. High resolution TEM image of 50 Å Zr silicate (12% Zr) on silicon substrate. The silicate film was annealed at 800 °C for 30 s in N_2 ambient. Zr silicate shows a single layer, amorphous structure, and sharp interface.

gate the compatibility of Zr silicate with poly silicon. We believe that Zr silicate should be even more compatible with polysilicon electrode.

In summary, Zr silicate films as an alternative gate dielectric prepared by comagnetron-reactive sputtering have been demonstrated. The dielectric constant of Zr silicate is directly related to the Zr concentration in the silicate film. Higher Zr concentration results in higher dielectric constant. But to prevent ZrO_2 or $ZrSiO_4$ precipitation, Si-rich film is preferred. The sputtered silicate film (12% Zr) shows low equivalent oxide thickness of 14.5 Å with a low leakage of 3.3×10^{-3} A/cm^2 at -1.5 V relative to flat band voltage. The silicate film remains amorphous and has a good interface with Si even after 900 °C rapid thermal annealing with the same equivalent oxide thickness.

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Yttrium silicate formation on silicon: Effect of silicon preoxidation and nitridation on interface reaction kinetics

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The effects of oxygen and nitrogen pretreatments on interface reaction kinetics during yttrium silicate formation on silicon are described. X-ray photoelectron spectroscopy (XPS) and medium energy ion scattering (MEIS) are used to determine chemical bonding and composition of films formed by oxidation of yttrium deposited on silicon. Capacitance–voltage testing is used to determine the quality of the dielectric and the electrical thickness. The effect of ultrathin silicon oxide, nitrided oxide, and nitrided silicon interfaces on metal oxidation kinetics is also described. When yttrium is deposited on clean silicon and oxidized, XPS and MEIS indicate significant mixing of the metal and the silicon, resulting in a film with Y–O–Si bonding and composition close to yttrium orthosilicate ($Y_2O_3 \cdot SiO_2$). A thin (~10 Å) *in situ* preoxidation step is not sufficient to impede the metal/silicon reaction, whereas a nitrided silicon interface significantly reduces the silicon consumption rate, and the resulting film is close to Y_2O_3. The mechanisms described for yttrium are expected to occur in a variety of oxide and silicate deposition processes of interest for high-k dielectrics. Therefore, in addition to thermodynamic stability, understanding the relative rates of elementary reaction steps in film formation is critical to control composition and structure at the dielectric/Si interface. © *2000 American Institute of Physics.* [S0003-6951(00)01741-1]

Advanced complementary–metal–oxide-semiconductor devices will require high dielectric constant (high-k) gate insulators to maintain sufficient capacitance and minimize tunneling. Physical vapor deposition (PVD) and chemical vapor deposition (CVD) of high-k materials (including Ta_2O_5, HfO_2, ZrO_2, Al_2O_3, Y_2O_3, and metal silicates) often results in lower-k interface layers[1–5] that result from unwanted reactions with the silicon substrate.[6] In the case of silicate deposition, the interface layer may not be directly visible, since the composition of the interface layer may be similar to the deposited layer. These interface reactions are generally not predicted from equilibrium thermodynamics of the Si and bulk metal oxide,[7] but result from the nonequilibrium nature of the deposition, where the relative rates and energetics of the individual elementary reaction steps, as well as thermodynamics, determine interface composition and structure. High-k CVD from metalorganic sources on clean Si involves breaking of a metal–ligand bond, chemisorption of the metal complex (likely forming metal–silicon bonds), and subsequent oxidation. Understanding the role of metal–silicon bonds and engineered interfaces on silicon consumption reaction kinetics is a critical issue for integration of high-k dielectrics with silicon.

In this work, dielectric films were formed by sputtering thin (25 Å) yttrium films onto clean and *in situ* modified silicon, then oxidizing in N_2O at 600–900 °C. The effects of interface oxidation and nitridation on silicon consumption during thermal oxidation of deposited yttrium are reported. Yttrium has a strong affinity for oxygen, and Y_2O_3 is expected to be stable on silicon at high temperature.[7] Materials were analyzed *ex situ* using x-ray photoelectron spectroscopy [(XPS) referenced to Si $2p$ at 99.3 eV] and medium-energy ion scattering (MEIS).[8] The MEIS compositions are reported as an average composition up to a depth of ~20 Å.

In the first experiment, 25 Å of yttrium is sputtered onto clean Si(100) and annealed at 600 °C in N_2O at 1 atm. XPS analysis of the resulting film (sample a) is shown in Figs. 1(a), 2(a), and 3(a) for the Y $3d$, O $1s$, and Si $2p$ regions, respectively. The Y $3d$ spectrum [Fig. 1(a)] shows a doublet due to spin-orbit splitting into the Y $3d_{3/2}$ and Y $3d_{5/2}$ components at 160.3 and 158.3 eV, respectively. The peak at 158.3 eV is higher than the 156.8 eV reported for Y $3d_{5/2}$ in Y_2O_3,[9] indicating that the oxidized layer has bonding struc-

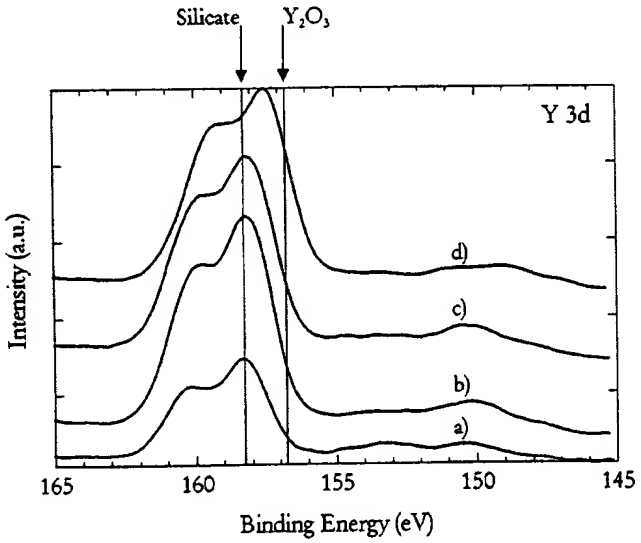

FIG. 1. Y $3d$ photoelectron spectra for films formed on: (a) silicon, (b) silicon oxide, (c) nitrided oxide, and (d) nitrided silicon. Nitrided silicon impedes silicon incorporation in the film causing the Y $3d$ peak to shift to lower BE.

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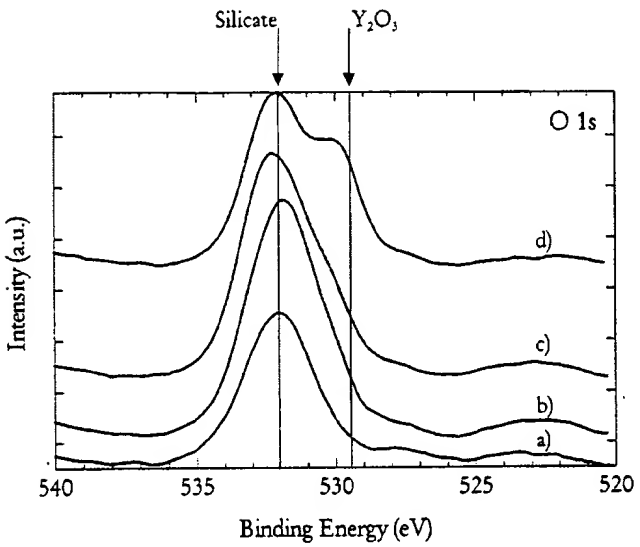

FIG. 2. O 1s photoelectron spectra for films formed on: (a) silicon, (b) silicon oxide, (c) nitrided oxide, and (d) nitrided silicon. The shoulder at 530.0 eV indicates an increase in O–Y–O bonding.

ture substantially different from Y_2O_3. The Y 3d spectra exhibit small features at ~150 eV that are assigned to a combination of the silicon substrate Si 2s peak, Si–O Si 2s peak, and the Y 3d satellite. No evidence for yttrium silicide bonds (Y $3d_{5/2}$ at ~155.8 eV)[10] is observed in any of the oxidized films discussed here. The O 1s peak at 532.0 eV is intermediate between O 1s for SiO_2 (533.0 eV) and Y_2O_3 (529.5 eV) and is broader than expected for either elemental oxide. The two peaks in the Si 2p spectrum [Fig. 3(a)] are assigned to silicon in the substrate (99.3 eV)[9] and silicon bound to oxygen in the film (102.2 eV), but the peak at ~102 eV lies between the silicon substrate peak and the expected peak position for SiO_2 (103.3 eV).[9] The chemical shifts in Figs. 1(a), 2(a), and 3(a) are consistent with a thin film containing a significant fraction of silicate (Y–O–Si) bonding units,[9] where electron density is donated from yttrium to neighboring Si–O bonds, in agreement with the

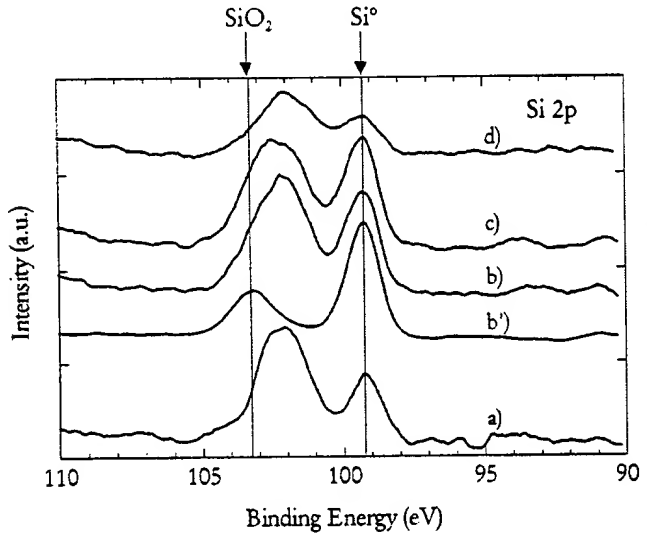

FIG. 3. Si 2p photoelectron spectra for films formed on: (a) silicon, (b) silicon oxide, (c) nitrided oxide, and (d) nitrided silicon. The spectrum for plasma oxidized silicon is presented as b′. For (a), (b), and (c), the peak at 102.2 eV is consistent with yttrium silicate.

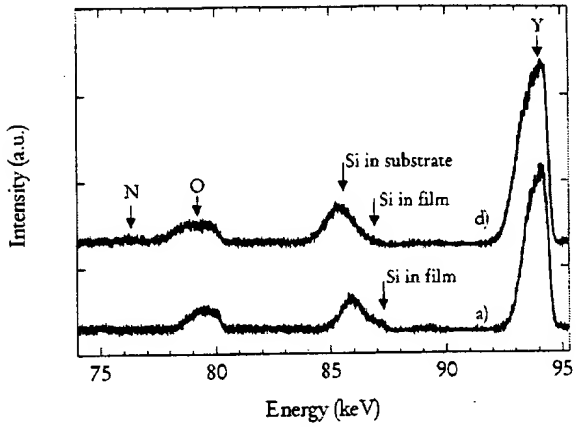

FIG. 4. MEIS energy spectra for films formed on: (a) silicon and (d) nitrided silicon. The shoulder at 87.0 keV representing silicon in the film is clearly larger for the film formed on (a) silicon than (d) nitrided silicon.

electronegativities of Y, Si, and O (1.2, 1.8, and 3.5 on the Pauling scale). MEIS results for sample (a) [Fig. 4(a)], show a high-energy (87.0 keV) shoulder on the silicon substrate peak, indicating Si in the film. The composition of this film calculated from the MEIS spectrum is $(Y_2O_3)_{0.58} \cdot (SiO_2)_{0.42}$. The XPS and MEIS data are consistent with the film being a yttrium orthosilicate ($Y_2O_3 \cdot SiO_2$) mixed with some additional Y_2O_3. Other stable yttrium silicates are also known,[11] with (Y_2O_3):(SiO_2) ratio <1. The absence of phase separated Y_2O_3 in the Y 3d XPS spectrum may be due to instrument sensitivity or to bond strain in the clustered Y_2O_3 network. Capacitance–voltage analysis of similarly prepared films indicates that good quality dielectric layers with equivalent oxide thickness of ~12 Å and dielectric constant in the range of 12–14 can be formed using this procedure.[12] As discussed below, the silicate structure likely results from relatively fast silicon diffusion into the metal leading to a metal silicide layer that is subsequently oxidized to form Y–O–Si bonds.

Various Si surface pretreatments were explored to modify and control the silicon/metal interaction and oxidation behavior. Pretreatments included plasma oxidation of silicon, plasma oxidation followed by nitridation, and plasma nitridation of silicon. Each of these steps were performed *in situ* using a remote N_2O or N_2 plasma source (N_2O^* or N_2^*, respectively).[12] Oxidation and nitridation conditions were controlled to attain ultrathin (~10 Å) pretreatment layers, as determined by XPS.[12] Each pretreatment was followed by *in situ* yttrium deposition (25 Å) and *ex situ* annealing at 600 °C in N_2O at 1 atm.

The oxidation pretreatment results in a ~10 Å SiO_2 layer with a well-defined Si–O feature at 103.3 eV, as shown in Fig. 3(b′). When yttrium is deposited on this surface and oxidized, the XPS spectra of the resulting film (spectra b in Figs. 1, 2, and 3) are indistinguishable from the film formed directly on silicon without the oxide pretreatment (sample a) with possibly a slight shift (~0.1 eV) to lower binding energy (BE). No evidence for the SiO_2 feature at 103.3 eV is observed in Fig. 3(b), indicating conversion of SiO_2 to silicate during oxidation. MEIS analysis (not shown) provides a composition of $(Y_2O_3)_{0.63} \cdot (SiO_2)_{0.37}$ indistinguishable, within experimental error (~0.04), from the clean Si case.

In the next experiment, a clean Si sample was oxidized

as above, then exposed to a remote N_2 plasma under conditions that resulted in ~1 monolayer of nitrogen at the SiO_2/Si interface. When yttrium is deposited on this nitrided oxide surface and oxidized as above, the Y 3*d* peak [Fig. 1(c)] is shifted to lower BE, and the O 1*s* peak [Fig. 2(c)] is shifted slightly to higher BE compared to the film formed directly on silicon. A slight shoulder at 530.0 eV (near the expected O 1*s* position for Y_2O_3) is observed in the O 1*s* spectrum of Fig. 2(c). No evidence for the SiO_2 feature at 103.3 eV is observed in Si 2*p* spectrum [Fig. 3(c)], again indicating conversion of SiO_2 to silicate during oxidation. MEIS yields a composition of $(Y_2O_3)_{0.72}\cdot(SiO_2)_{0.28}$, indicating that the silicon fraction is reduced compared to the film formed on clean silicon. This is consistent with the nitrogen slowing the interaction between the silicon substrate and the deposited metal, with the SiO_2 layer still available for reaction with the metal.

The fourth sample consists of the clean Si being exposed only to the N_2^* pretreatment prior to yttrium deposition and oxidation. The resulting oxidized yttrium film is significantly different than when the starting surface is clean or oxidized silicon. For the oxidized yttrium film on N_2^*-treated silicon, the Y 3*d* peak [Fig. 1(d)] is shifted 0.8 eV to lower BE compared to films formed on clean or oxidized Si [Figs. 1(a) and 1(b), respectively], and the O 1*s* spectrum [Fig. 2(d)] exhibits a strong shoulder at 530.0 eV. For Y_2O_3, Y $3d_{5/2}$ is at 156.8 eV and O 1*s* is at 529.5 eV compared to 158.2 and 532 eV, respectively, for the silicate formed on clean Si. The chemical shifts for the film formed on nitrided silicon are consistent with the dielectric layer having composition close to Y_2O_3. Figure 4 shows MEIS results for dielectric films formed on N_2^*-treated surfaces (spectrum d), compared to those formed on clean silicon (spectrum a). For spectrum d, a signal due to interface N is observed at ~76 keV, consistent with ~1 monolayer of nitrogen localized at the silicon/dielectric interface after yttrium deposition and oxidation. In spectrum a, a signal at 87.0 keV is clearly seen due to Si in the film, indicating significant mixing of metal and silicon before or during the oxidation process. Samples with oxidation and oxidation/nitridation pretreatments show MEIS spectra qualitatively similar to spectrum a, indicating Si mixing with the metal. However, in spectrum d, corresponding to the N_2^*-treated silicon, the silicon signal at 87.0 keV is nearly indiscernible and the composition is Y_2O_3 with ~27% yttrium silicate consistent with the XPS results.

It is well known that at relatively low temperature, silicon will readily interdiffuse with some metals, including Hf, Zr, La, and Y[13,14] to form silicides. The above results indicate that when yttrium (which forms a silicide and a stable oxide) is deposited onto silicon and oxidized, the silicon diffuses to form a silicide,[13,14] and subsequent oxidation results in a layer with significant silicate composition (sample a in Figs. 1–4). This intermixing also occurs when the surface is oxidized before metal deposition. Because yttrium has a very high affinity for oxygen, annealing results in reduction of the available silicon oxide, leading to a silicate layer (i.e., samples b and c in Figs. 1–3). When ~1 monolayer of nitrogen is present at the interface, the silicon diffusion from the substrate is impeded. Any silicon oxide on top of the N layer will still react with the metal to form a silicate (spectra c in Figs. 1–3). However, when only nitrided silicon is present (spectra d in Figs. 1–4), oxidation of deposited metal results in a structure closer to pure metal oxide, consistent with impeded silicon diffusion through the nitrided layer. These reactions are demonstrated here for the case of yttrium, but similar results are expected for other metals that form silicides and stable oxides on silicon including Hf, Zr, La, etc. Elementary reaction steps in metal oxide CVD will also include metal–silicon bond formation and oxidation, so similar mechanistic processes described here for PVD films are expected in CVD processes, and these mechanisms are likely responsible for interface layers commonly observed in these systems. This demonstrates that, in addition to thermodynamic stability of the metal oxide, the relative energetics and rates of the elementary reaction steps in film formation are critical for controlling composition and structure at the dielectric/Si interface.

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Microscopic model for enhanced dielectric constants in low concentration SiO_2-rich noncrystalline Zr and Hf silicate alloys

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Dielectric constants, k, of Zr(Hf) silicate alloy gate dielectrics obtained from analysis of capacitance–voltage curves of metal–oxide–semiconductor capacitors with 3–6 at. % Zr(Hf) are significantly larger than estimates of k based on linear extrapolations between SiO_2 and compound silicates, $Zr(Hf)SiO_4$. Analysis of infrared spectra of Zr silicate alloys with 3–16 at. % Zr indicates increases in the coordination of Zr to O atoms from 4 to approximately 8 with increasing Zr content. The major contributions to enhancements in k in these low Zr(Hf) content alloys are explained by a transverse infrared effective charge that scales *inversely* with increasing Zr–O bond coordination. © *2000 American Institute of Physics.* [S0003-6951(00)01344-9]

There is considerable interest in replacement dielectrics for SiO_2 in metal–oxide–semiconductor (MOS) devices with channel lengths <100 nm. Scaling requires a gate dielectric capacitance *equivalent* to a SiO_2 thickness of <1.5 nm, a regime where direct tunneling exceeds 1–5 A/cm^{-2} at operating biases, and is too high for many mobile applications.[1] Insulators with higher dielectric constants offer potential for increased capacitance in physically thicker films, providing a possible way to reduce direct tunneling.[2] MOS capacitors with SiO_2-rich Zr and Hf silicates with 3–6 at. % Zr(Hf) have been reported to have increased dielectric constants and reduced tunneling currents.[1,3–5] Reported values of k from capacitance–voltage curves are ~8–11, and more than 50% larger than values estimated from a linear extrapolation of k between SiO_2, ~3.9, and the compound silicates, ~12 (Fig. 1). These *enhanced* values of k can not be reconciled with macroscopic dielectric theory that predicts a downward bowing between end members in a mixed materials system.[6] Since macroscopic theory applies to mixtures in which chemical bonding of constituents does not change with composition, it is important to determine if SiO_2-rich Zr(Hf) silicate alloys satisfy this condition.

Chemical bonding in Zr silicates ($[ZrO_2]_x[SiO_2]_{1-x}$) has been studied by Fourier-transform infrared spectroscopy, (FTIR);[7] similar bonding is expected in Hf silicates. Figure 2 displays absorbance for Zr silicate films prepared by remote plasma enhanced chemical vapor deposition.[2,7] Alloy compositions were determined to ±0.05 by Rutherford backscattering spectrometry. Spectra of as-deposited films and films annealed for 30 s in Ar at temperatures to 800 °C (not shown) are essentially the same, whereas spectra of films annealed at 900 °C are markedly different. Features in as-deposited films with x~0.1 and 0.23 are assigned to Si–O–Si groups in *corner-connected* arrangements, as stretching modes at ~1150, 1065, and 810, and a rocking mode at ~450 cm^{-1}.[7,8] Two other features are assigned to Si–O–Zr stretching vibrations, a terminal Si–O mode at ~950 cm^{-1} that is a shoulder on the 1065 cm^{-1} absorption, and a broader Zr–O feature at ~450 cm^{-1} that is *accidentally* degenerate with the Si–O–Si rocking mode. Since both stretching modes involve predominantly O-atom motion, their frequencies reflect a significantly smaller force constant for the Zr–O vibration. This results from a Zr–O bond length of 0.22 nm compared to ~0.16 nm for Si–O.[9] Far-IR spectra to 50 cm^{-1} show no additional features. Spectral features in an as-deposited x~0.5 film are assigned to a random close packing of Zr^{4+} and SiO_4^{4-} ions.[7,8] The 800–1200 cm^{-1} band includes SiO_4^{4-} vibrations, and the ~450 cm^{-1} band is dominated by Zr–O vibrations. After a 900 °C anneal, spectral changes at all compositions indicate a chemical phase

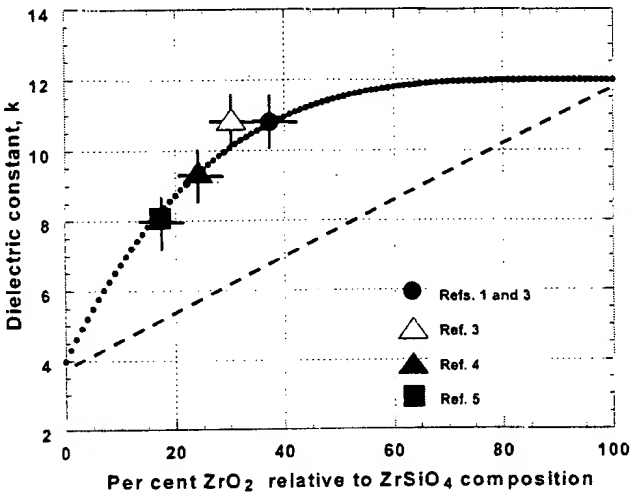

FIG. 1. The dotted curve indicates the dielectric constant calculated from Eq. (3) as a function of the percent $Zr(Hf)O_2$ relative to the stoichiometric silicate compound composition, $Zr(Hf)SiO_4$. Experimental points are from Refs. 1, 3, 4, and 5. The dashed line is a linear extrapolation between the dielectric constant of SiO_2 and a nominal dielectric constant of 12 for $Zr(Hf)SiO_4$.

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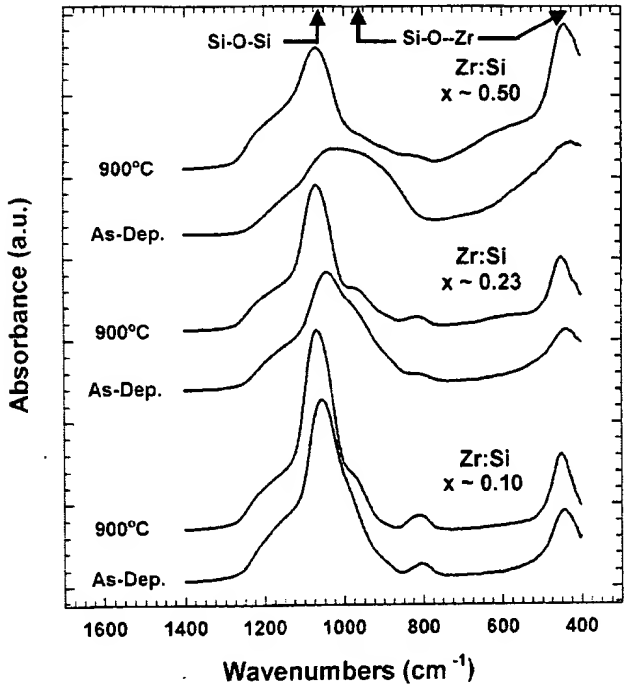

FIG. 2. Absorbance vs wave number for three Zr silicate alloys with different ratios of Zr:Si, as-deposited and after a 30 s, 900 °C anneal in Ar.

separation into (i) a noncrystalline low Zr-content silicate alloy with ~1–2 at. % Zr and (ii) noncrystalline (x~0.1 and ~0.23) or crystalline ZrO_2 (x~0.5).[7]

As in bulk silicate glasses, introduction of oxides of electropositive Zr(Hf) atoms into SiO_2 results in a breakup or *modification* of the network structure.[10,11] Homogeneity in bulk silicate glasses quenched from high temperatures is limited by chemical phase separation, and in many instances homogeneous glasses are obtained only at relatively low metal oxide content, <5–10 mol %. This is not a limitation in thin film silicates deposited at temperatures <500 °C.[1–5,7] The analysis below applies to these films, as well as those prepared at low temperatures, and subsequently processed at temperatures <800 °C. Capacitors with Zr(Hf) silicate dielectrics in Refs. 1, 3, 4, and 5 meet these temperature constraints. Introduction of a $Zr(Hf)O_2$ *molecule* into the SiO_2 network is assumed to break two Si–O bonds,[11] so that the concentration of terminal Si–O terminal bonds is linear in Zr composition. The coordination of silicon to oxygen remains 4, and there are five tetrahedral groups with different distributions of O atoms that are (i) connected to the network through *bridging* Si–O–Si bonds, or are (ii) in *terminal* Si–O groups. Figure 3 gives the fractional concentrations of these groups in Zr(Hf) silicates alloys as a function of composition as obtained from the following expression:

$$(w+z)^4 = w^4 + 4zw^3 + 6z^2w^2 + 4z^3w + z^4 = 1, \qquad (1)$$

where w is the fraction of bridging O atoms, and $z = 1 - w$ is the fraction of terminal O atoms.

In alloys with x<0.1, Zr atoms (or Zr^{4+} ions) are incorporated predominantly as network modifiers with four terminal negatively charged O-atom neighbors in *corner-connected* arrangements[11] (Fig. 4). As the mole fraction of ZrO_2 is increased, an increasing fraction of these groups have two or more terminal Si–O bonds. This causes the coordination of Zr atoms to increase above 4 including both *edge-* and *corner-connected* arrangements. In crystalline silicates, Zr^{4+} ions have a coordination of 8, with each Zr-atom making *edge and corner connections* to SiO_4^{4-} tetrahedra.[2,4] This same bonding coordination of 4 for Si and 8 for Zr(Hf) is assumed for the amorphous compound silicates.

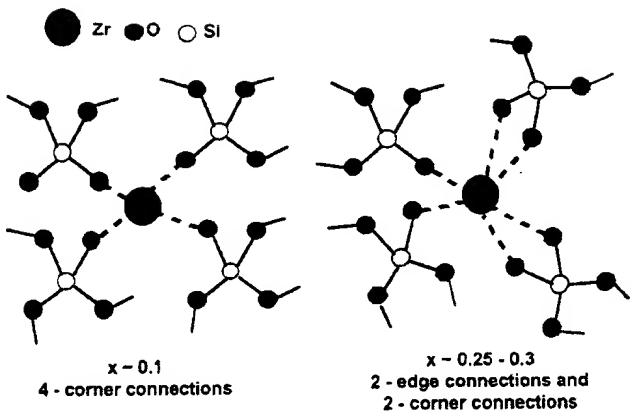

FIG. 3. Relative fractions of five tetrahedral silicon-oxygen bonding groups with different numbers of bridging and terminal oxygen atoms plotted as a function of the percent of $Zr(Hf)O_2$ relative to the stoichiometric silicate compound composition, $Zr(Hf)SiO_4$.

The contribution of a vibrational mode to the dielectric constant is proportional to the square of its transverse infrared effective charge, e_T^*, and is different for different bonding coordinations of the same atom pair.[9,13] The FTIR spectra of Fig. 2 indicate a broadening of the 950 cm^{-1} feature with increasing x. Based on Fig. 3, the broadening occurs at alloy concentrations where the Zr-atom coordination and ratio of *edge-* to *corner-connected* arrangements has increased. If e_T^* scaled directly with increases in the number of terminal Si–O bonds, this broadening would have been accompanied by a marked increase in absorbance of the 950 cm^{-1} feature relative to the network Si–O–Si spectral peak at 1065 cm^{-1}. To the contrary, FTIR results indicate the relative absorbance of terminal Si–O groups does not scale in this way, and

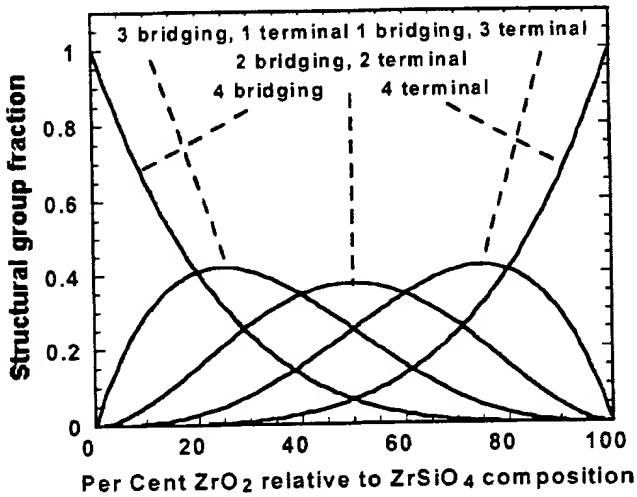

FIG. 4. Transition in local bonding arrangements of Zr atoms in Zr silicate alloys from low to high ZrO_2 concentrations. At low concentrations the dominant bonding arrangements are between the Zr atoms and four terminal O atoms in a *corner-connected* geometry. At higher concentrations (fraction of ZrO_2>30%–35%), there is a transition to bonding including more than one O atom in *edee-connected* arrangements.

therefore the absorbance *decreases* with increasing Zr coordination. The *bond order* for a Zr–O bond is defined as the ratio of number of valence electrons available from each Zr atom (4) to the number of O-atom nearest-neighbors. Based on this definition, four-fold coordinated Zr atoms have the largest bond order, 1. They also have the highest degree of covalency,[12] so that dynamic contributions to e_T^* are larger than for higher bonding coordinations in which bond order is reduced and bonding becomes more ionic.[9,13] Scaling of local properties such as bond energies and stretching force constants with bond order is well established.[12] Consistent with the relative absorption strengths of single, double, and triple carbon-oxygen bonds, this scaling can be extended to e_T^*. Since the contributions of infrared active modes to k are proportional to $(e_T^*)^2$, the appropriate scaling variable is the square of the bond order. There is also an additional and smaller contribution to the dielectric constant from electronic transitions that is included in the end-member constants of the scaling relationship given later.

Based on Eq. (1) and an assumption that contribution of Zr–O bonds to the dielectric constant scales quadratically with Zr–O bond order, the variation of k with alloy composition is approximated by

$$k \sim 3.9w^4 + 12(4a_{1,3}zw^3 + 6a_{2,2}z^2w^2 + 4a_{3,1}z^3w + a_{4,4}z^4), \tag{2}$$

where the first term is the contribution to k from Si–O–Si bonding, and the second term is from Si–O–Zr bonding. The constants 3.9 and 12 fix the end-member values.[1,4] Combining Eq. (2) with Eq. (1), the following relationship is obtained:

$$k \sim 3.9 + 8.1(4a_{1,3}zw^3 + 6a_{2,2}z^2w^2 + 4a_{3,1}z^3w + a_{4,4}z^4); \tag{3}$$

$a_{i,j}$ are the product of (i) the number of terminal Si–O bonds per group, and (ii) the square of an average bond order. The $a_{i,j}$'s are approximated by $a_{1,3} \sim 1x(4/4)^2 = 1$, $a_{2,2} \sim 2x[4/(5-6)]^2 \sim 1.05$, $a_{3,1} \sim 3x[4/(6-7)]^2 \sim 1.15$, and $a_{4,4} \sim 4x(4/8)^2 = 1$, and are of order 1. The curve in Fig. 1 is for $a_{i,j} = 1$. Values of $a_{2,2}$ and $a_{3,1} > 1$ would increase k for alloys with more than 45%–50% ZrO_2 relative to $ZrSiO_4$ (or $x > 0.25$). Since values of k for Zr(Hf) content >7 at. % have not been reported, the application of the model is restricted to alloys with lower concentrations. The experimental data from Refs. 1, 3, 4, and 5 with alloy content <7 at. % Zr fall close to calculated curve indicating that the empirical relationship of Eq. (3) provides a quantitative description of enhanced dielectric constants for alloys in this composition range. A similar enhancement in the index of refraction, or equivalently the optical frequency dielectric constant, is also expected to occur in low Zr(Hf) content silicate alloys. Our initial experiments have indicated that this enhancement is present, and that it also scales with the square of the bond order. In the spirit of the analysis presented above, this contribution is *implicitly included* in the constant and $a_{i,j}$ terms of Eq. (3).

It has been shown that the enhanced dielectric constants of the SiO_2-rich Zr and Hf silicates are due primarily to the four-fold coordination of the Zr(Hf) atoms in the alloy composition range below about 7 at. %. Similar enhancements in k at low metal-atom concentrations are also expected for SiO_2-rich silicate alloys with (i) TiO_2, (ii) $Y(La)_2O_3$ for compositions up to the *first* silicate phase, $La(Y)_2SiO_5$,[14] and (iii) oxides of other polarizable atoms such as Pb, Bi, Tl, etc. Chemical bonding at Si-silicate alloy interfaces should be similar to Si–SiO_2 interfaces, so that in addition to providing significantly increased capacitance and reduced direct tunneling, incorporation of these silicate alloys into MOS devices should yield interface properties and reliabilities similar to those of devices with SiO_2 dielectrics.

Note added in proof: As-deposited Zr silicate alloys with values of x from 0.1 to 0.8 were studied by extended x-ray absorption fine structure spectroscopy (EXAFS). Analysis of EXAFS data confirmed the increases in Zr atom coordination with increasing ZrO_2 content that have been discussed in the text. The coordination of Zr increased from 4.5±1 for an $x \sim 0.1$ (or ~3.3 at. % Zr) alloy to 7.2±1 for samples with $x \sim 0.25$ (or ~8.3 at. % Zr), spanning the range in which the dielectric constant enhancement is decreasing (see Fig. 1). In addition, analysis of the EXAFS data indicated two Zr-O nearest neighbor distances of 0.21 and 0.23 nm, approximately equal to the two Zr-O bond-lengths in the crystalline $ZrSiO_4$ phase.

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Characterization of RuO_2 electrodes on Zr silicate and ZrO_2 dielectrics

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The rutile stoichiometric phase of RuO_2, deposited via reactive sputtering, was evaluated as a gate electrode on chemical vapor deposited ZrO_2 and Zr silicate for Si–p-type metal–oxide–semiconductor (PMOS) devices. Thermal and chemical stability of the electrodes was studied at annealing temperatures of 400, 600, and 800 °C in N_2. X-ray diffraction was measured to study grain structure and interface reactions. The resistivity of RuO_2 films was 65.0 $\mu\Omega$ cm after 800 °C annealing. Electrical properties were evaluated on MOS capacitors, which indicated that the work function of RuO_2 was ~5.1 eV, compatible with PMOS devices. Post-RuO_2 gate annealing up to 800 °C, resulted in only a 1.4 Å equivalent oxide thickness ($T_{ox\text{-}eq}$) change and 0.2 V flatband voltage change for Zr silicate and a 4 Å $T_{ox\text{-}eq}$ change for ZrO_2 dielectrics. Tantalum electrodes were also studied on ZrO_2 as a comparison of the stability of RuO_2 electrodes. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1347402]

As silicon complementary metal–oxide–semiconductor (CMOS) devices are scaled below 100 nm, advanced high-K gate dielectrics will be required to obtain oxide equivalent thickness $T_{ox\text{-}eq}$ <1.0 nm. As $T_{ox\text{-}eq}$ decreases, polycrystalline silicon (poly-Si) depletion problem becomes severe, making it necessary to consider alternative gate electrodes, such as metals.[1] The search for metal gates faces many challenges such as (a) compatible work functions (~4 eV for n-type MOS and ~5 eV for p-type MOS), (b) process compatibility, and (c) thermal/chemical interface stability with dielectrics.

Recently, several studies have been performed on ZrO_2, HfO_2, and their silicates.[2,3] ZrO_2 is attractive because of its high dielectric constant (~25), reasonable energy band gap (~5 ev), and high stability. The gate electrode can also impact the electrical and physical properties of the gate dielectric. For example, it was reported that poly-Si deposition at higher temperatures (620 °C) results in the reduction of ZrO_2 to form a Zr-rich layer near the poly-Si/ZrO_2 interface, leading to very high leakage currents.[4] In most of the recent studies, gold and platinum have been used as stable gate electrodes, however, several issues such as cost, film stress, and lithography limit their attractiveness. Therefore, selecting a compatible gate electrode for high-K dielectrics is a very important and challenging task.

Thin films of transition conducting metal oxides such as ruthenium oxide, RuO_2, and iridium oxide, IrO_2, are attractive gate electrodes since they have large workfunctions (~5 eV), low resistivity and excellent thermal stability.[5,6] These films have been studied as diffusion barriers between Al and Si,[7] in ferroelectric thin film capacitors for dynamic random access memories and in ferroelectric nonvolatile memories.[8] However, most of the reported work has not evaluated the high temperature (>700 °C) stability of RuO_2 and IrO_2. It should also be mentioned that RuO_2 can form a volatile and toxic species, RuO_4, if annealed at 900 °C either in high vacuum or high oxygen containing ambients[9] and care should be taken to avoid annealing RuO_2 in these environments. We have recently evaluated RuO_2 films on SiO_2 and have found excellent electrical properties with good thermal stability, high carrier concentration, and good breakdown characteristics.[10] In this letter, we evaluate the electrical and thermal stability of RuO_2 on ZrO_2 and Zr silicate and compare them to other well-known gate electrodes such as Ta and TaN.

The substrates used in this work were (100) Si wafers with active areas defined by 3500 Å field oxidation. A 100 Å sacrificial oxide was grown to improve the Si surface and was removed prior to gate dielectric deposition. ZrO_2 and Zr-silicate thin films were directly deposited on Si substrate by rapid-thermal metalorganic chemical vapor deposition using zirconium tertiarybutoxide ($C_{16}H_{36}O_4Zr$) as the Zr precursor at the University of Texas. It should be noted that deposition technique can have a large impact on film properties and films deposited under various techniques may have differing results. No postoxide deposition annealing was performed prior to gate electrode deposition. RuO_2 thin films were deposited using a rf magnetron sputtering system as described in our previous work.[10] A Sloan Dectak profilometer was used to measure the thickness of films and the thickness of all films was in the range of 50 nm. The RuO_2 gates were patterned using lift-off lithography. The samples were then annealed at temperatures of 400, 600, and 800 °C in N_2 for 40 min. The crystal structure of the RuO_2 films was determined by x-ray diffraction (XRD). Electrical resistivity was measured by the Van Der Pauw four-probe method. Capacitance–voltage (C–V) and current–voltage characteristics were obtained using HP4284A and HP4155, respectively.

X-ray analysis of the as-deposited films did not show

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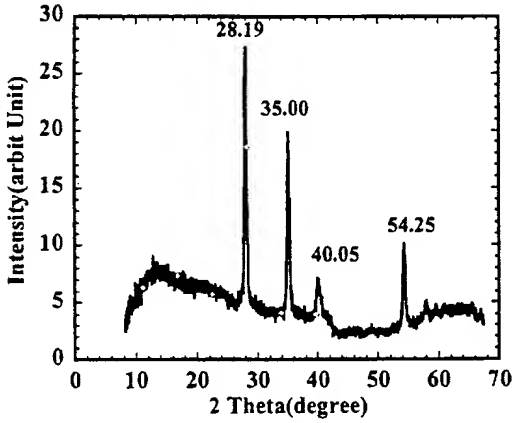

FIG. 1. X-ray diffraction of RuO_2 film after 600 °C annealing.

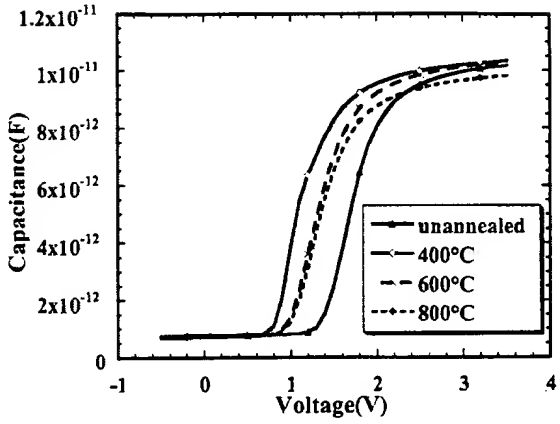

FIG. 2. $C-V$ curves of capacitors of Zr silicate with RuO_2 electrode at frequency 1 MHz before and after 400, 600, and 800 °C annealing.

any x-ray diffraction peaks within a scanning angle from 0° to 70° of 2θ. Therefore, the as-deposited films were assumed to be nanocrystalline in nature. After 600 °C annealing in N_2 for 30 min, XRD patterns were obtained and are shown in Fig. 1. The diffraction peaks in the XRD pattern shown matches the crystal rutile stoichiometric phase of RuO_2. The narrow width of the peaks points to a reasonably large grain microstructure. It is obvious that the grain size of RuO_2 films increase with increasing annealing temperature.[11] This has also been confirmed by resistivity measurements (shown in Table I) which showed that resistivity decreased as anneal temperature increased. A breakdown study on capacitors with RuO_2 electrode on SiO_2 dielectric after various anneal temperatures did not reveal any significant differences in reliability indicating that the growth of grains did not negatively impact the dielectric interface properties.[10] The resistivity of RuO_2 after 800 °C annealing was 65 $\mu\Omega$ cm which is considerably lower than heavily doped polysilicon.

Figure 2 shows the $C-V$ curves of the capacitors with RuO_2 gate electrodes on Zr-silicate dielectric before and after 400, 600, and 800 °C annealing in N_2 for 40 min. The capacitance was measured at a frequency of 1 MHz on an area equal to 0.9×10^{-5} cm^2. The flat-band voltage (V_{FB}) and $T_{ox\text{-}eq}$ for the capacitors were obtained by using NCSU CV program[12] which enables us to extract the work function. Before annealing, the V_{FB} voltages are shifted due to sputtering damage caused during electrode deposition. After 400 °C annealing, $T_{ox\text{-}eq}$ was close to the unannealed case of 2.73 nm and the V_{FB} was 1.01 V. The work function value obtained from this V_{FB} is ~5.1 eV and closely matches our previous RuO_2 workfunction of 5.04 eV obtained on SiO_2 dielectrics.[10] Also, the work function value obtained using MOS capacitors is slightly higher than those obtained using photoemission[13] and may relate to the difference in the measurement techniques.

After 600 °C annealing, V_{FB} changed to 1.26 V but $T_{ox\text{-}eq}$ still remained close to 2.7 nm. A change in V_{FB} of ~0.2 V is attributed to negative fixed charges that are created in the dielectric after annealing. The creation of negative fixed charges in Zr containing dielectrics with inert electrodes (Au) has also been reported by Houssa *et al.*[14] Moreover, as shown in Table I, RuO_2 annealing up to 800 °C on SiO_2 dielectrics did not change the V_{FB} indicating that RuO_2 was not degrading the dielectric. Further annealing at 800 °C resulted in insignificant change of $T_{ox\text{-}eq}$ and V_{FB}. This data, which is summarized in Table I, indicates that RuO_2 gate electrodes exhibit reasonable thermal stability on Zr silicate.

Figure 3 shows the $C-V$ measurement of RuO_2 gate electrodes on ZrO_2 gate dielectrics before and after a 400, 600, and 800 °C anneal in N_2 for 40 min. As shown, there is a V_{FB} shift before annealing due to sputtering damage similar to Zr silicate and SiO_2. This damage is removed after a 400 °C anneal and the proper work function of RuO_2 again is obtained with no change in $T_{ox\text{-}eq}$. After 600 °C annealing, there is an increase in $T_{ox\text{-}eq}$ of 4 Å and a reduction in gate current owing to the increase in resistivity of the dielectric.[4] In this case, no change in V_{FB} is observed upon annealing. A

TABLE I. Equivalent oxide thickness and flatband voltages before and after annealing for capacitors with Zr-silicate dielectrics and SiO_2.

Process condition	RuO_2 resistivity ($\mu\Omega$ cm)	$T_{ox\text{-}eq}$ (nm)		V_{FB}(V)	
		Zr silicate	SiO_2	Zr silicate	SiO_2
Before anneal	500.3	2.69	3.90	1.64	1.77
400 °C anneal	117.8	2.73	3.90	1.01	0.98
600 °C anneal	81.6	2.73	3.90	1.26	1.00
800 °C anneal	65.0	2.84	4.00	1.28	1.08

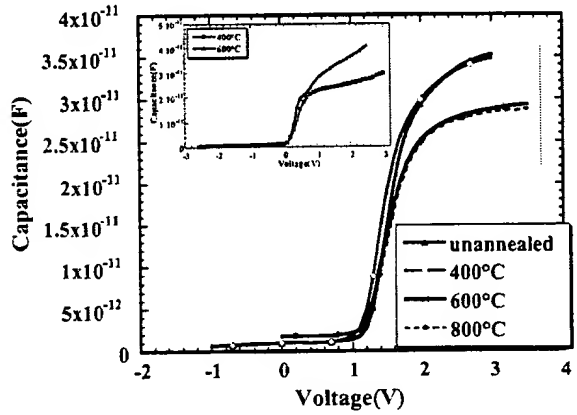

FIG. 3. $C-V$ curves of capacitors of ZrO_2 with RuO_2 electrode at frequency 1 MHz before and after 400, 600, and 800 °C annealing. The inset shows $C-V$ curves of capacitors of ZrO_2 with Ta electrode at frequency 1 MHz after 400 and 600 °C annealing. Area of capacitor=2.5×10^{-5} cm^2.

subsequent 800 °C anneal does not further change the $T_{ox\text{-}eq}$ or V_{FB} of the device. This data suggests that RuO_2 gate electrodes also exhibits reasonable thermal stability on ZrO_2.

We have also evaluated other common metals to compare their stability on ZrO_2 to that of RuO_2. The inset of Fig. 3 shows the $C-V$ characteristics of Ta gates on ZrO_2 dielectric after a 400 and 600 °C anneal. As shown, the Ta gate exhibits large instabilities on ZrO_2 even at 600 °C indicating that Ta has reacted with the dielectric causing a capacitance and a V_{FB} change. The results with TaN gates (not shown), are slightly better than Ta, but still exhibit less than acceptable change of the $C-V$ characteristics.[15] Severe degradation was also observed with Zr, Hf, and TiN gates.[16,17] Compared to these electrodes, RuO_2 exhibits significantly better stability on both ZrO_2 and Zr silicate even up to 800 °C.

Metal stability on dielectrics can be predicted via thermodynamics, and metals whose oxides have high negative Gibbs free energy of formation will tend to reduce the dielectric underneath. For example, Zr is very unstable on SiO_2 and takes up its oxygen by reducing it.[16] Similar reactions occur for Ta, Ti, Hf, V, etc.[17] It has also been shown that oxygen solubility is an indicator of instability, and metals with high oxygen solubility can result in redistribution of oxygen in the dielectric.[16] For example, Zr on ZrO_2, Ti on TiO_2, and Ta on Ta_2O_5 result in a single MO_x layer with a uniform distribution of oxygen upon low temperature annealing.[18]

The stability of the oxide thickness and flatband voltage on both Zr silicate and ZrO_2 suggests that RuO_2 gate electrodes are stable at least up to the temperatures studied here (800 °C). With the knowledge of the stable binary phases, it can be shown via thermodynamic calculations that Gibbs free energy of formation for RuO_2 is less negative than ZrO_2 thereby indicating that ZrO_2 will not be reduced under equilibrium conditions. Furthermore, since RuO_2 is an excellent oxygen diffusion barrier[19] (i.e., poor oxygen sink) it prevents oxygen loss from ZrO_2. The thermal stability of these films observed in this work is attributed to the excellent oxygen diffusion barrier and low oxygen solubility properties of RuO_2. On the other hand, metals such as Ta and Zr have high oxygen solubilites and also high negative Gibbs energies for oxide formation. Therefore, these metals can easily reduce ZrO_2 dielectrics resulting in a thinning of the dielectric as is evident by the capacitance increase after 600 °C annealing.

The slight decrease in capacitance of ZrO_2 and Zr-silicate dielectrics with RuO_2 gates after annealing can be attributed to the oxidation of the Si substrate. One possible source of this oxygen is the dielectric itself. Khawaja *et al.* found excess oxygen due to the embedded in the films during deposition and absorbed water in zirconium oxide by Rutherford backscattering and x-ray photoelectron spectroscopy.[20] It should be noted that the deposition technique can affect the levels of oxygen contained within the dielectric and it is expected that ZrO_2 deposited using other techniques (such as PVD, ALD, etc.) may have slightly different ΔV_{FB} and $\Delta T_{ox\text{-}eq}$ dependence on anneal conditions. Another source of oxygen could be attributed to the RuO_2 sputtering process where oxygen may accumulate in the dielectric. In either case, this oxygen is not believed to be a continuous source because the increase in capacitance saturates after 600 °C anneal for ZrO_2 indicating that this gate stack is a sealed system not allowing any additional oxygen to enter from the ambient. This is also consistent with the excellent oxygen diffusion barrier properties of RuO_2. The higher change in capacitance for ZrO_2 compared to Zr silicate may be related to the very high oxygen diffusion coefficients in ZrO_2 films.

In summary, we have demonstrated that RuO_2 gates on ZrO_2 and Zr silicate provide good thermal stability resulting in minimal change of V_{FB} and equivalent oxide thickness. The behavior of RuO_2 was in stark contrast to Ta gates which indicated instability at temperatures <600 °C. The stability of RuO_2 gates was attributed to its excellent oxygen diffusion barrier properties and its low Gibbs energy of formation compared to ZrO_2. This prevents oxygen loss from the dielectric thereby maintaining its electrical performance. It should be noted that RTAs can be used to further minimize the capacitance and flatband voltage shifts due to lower thermal budget. In conclusion, the stability of RuO_2 gates may enable high-K gate dielectrics and metallic electrodes to be implemented in advanced CMOS devices.

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Stability of zirconium silicate films on Si under vacuum and O_2 annealing

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The effect of postdeposition annealing in vacuum and in dry O_2 on the atomic transport and chemical stability of chemical vapor deposited $ZrSi_xO_y$ films on Si is investigated. Rutherford backscattering spectrometry, narrow nuclear resonance profiling, and low energy ion scattering spectroscopy were used to obtain depth distributions of Si, O, and Zr in the films. The chemical environment of these elements in near-surface and near-interface regions was identified by angle-resolved x-ray photoelectron spectroscopy. It is shown that although the interface region is rather stable, the surface region presents an accumulation of Si after thermal annealing. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1367288]

There is an impetus to replace SiO_2 as the gate dielectric in complementary metal oxide semiconductor (CMOS) transistors, since the exponential increase in tunnel current with decreasing film thickness sets a fundamental limit on the scaling of gate oxides.[1,2] The trend in reducing lateral dimensions of devices brings as a consequence a reduction of the capacitance of the involved MOS structures, thus calling for a higher dielectric constant and/or thinner films to compensate. Therefore, to keep device areas small and prevent leakage current while maintaining the same gate capacitance, a thicker film made with a material of higher dielectric constant (high-K) is required. Further mandatory requirements are: a sharp interface with Si substrate which would favor a low density of interface states; and physico-chemical stability at both the gate electrode/high-K dielectric and the high-K dielectric/Si–substrate interfaces in further processing steps. Previous investigations[3–8] indicated that a postdeposition annealing at moderate temperatures of thin films of different proposed dielectrics on Si may reduce the leakage current and the density of interface states down to acceptable levels of less than $10^{-11}/cm^2\,eV$. This was achieved in many cases without a significant lowering of the dielectric constant due to formation of intermediate SiO_2 layers.

Recent publications[4,5,7] showed that Zr silicates ($ZrSi_xO_y$), which are stable in direct contact with Si,[9] are good candidates for alternative, high-K dielectrics.

We report on atomic transport and chemical stability of $ZrSi_xO_y$ films submitted to post-deposition thermal anneals in a vacuum and in dry O_2. Zr silicate films, ~9 nm thick, were deposited by low pressure chemical vapor deposition at 650 °C. The postdeposition anneals were performed *ex situ* at 600 °C for 30 min, either in high vacuum ($P = 10^{-5}$ Pa) or in 7×10^3 Pa of dry O_2 98.5% enriched in the ^{18}O isotope ($^{18}O_2$). Annealing in isotopically enriched O allows distinguishing O eventually incorporated from that previously existing in the silicate films.

Zr profiles and areal densities were determined by Rutherford backscattering spectrometry (RBS) of 700 keV He^+ ions, detected at a scattering angle of 165° and tilting the sample by 70°. The depth resolution for Zr profiling obtained with this geometry is ~2 nm. RBS geometry and spectra for as-deposited and annealed samples are shown in Fig. 1(a), indicating a uniform and stable (after thermal annealing) distribution of Zr within the silicate film and sharp interfaces with the Si substrate. Areal densities of ^{16}O, ^{18}O,

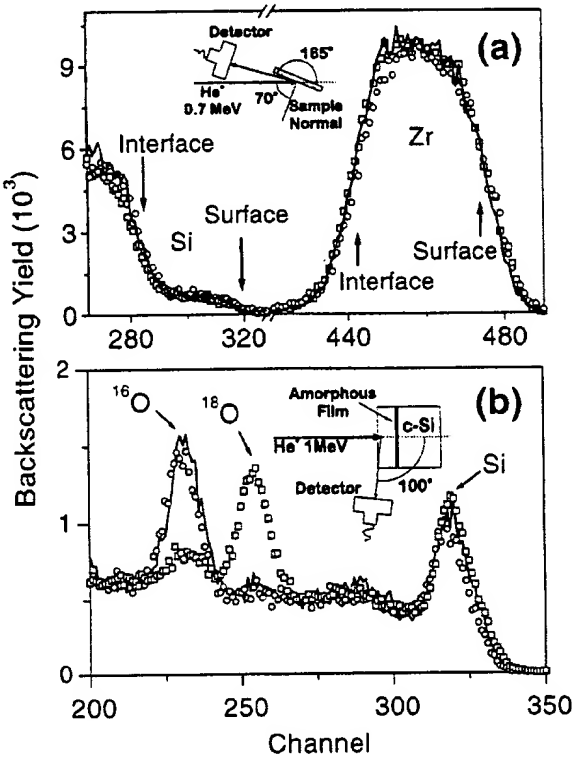

FIG. 1. (a) Zr and Si signals in RBS spectra of 700 keV incident He^+ ions; (b) channeled-RBS and grazing angle detection spectra of 1 MeV incident He^+ ions. The geometries are shown in the insets. Solid lines represent the as-deposited sample, empty circles and squares represent the vacuum- and $^{18}O_2$-annealed samples, respectively.

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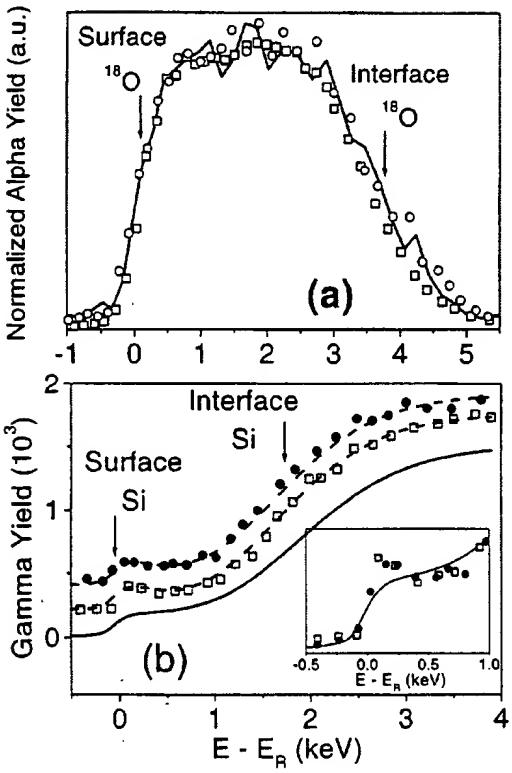

FIG. 2. (a) Normalized excitation curves of the nuclear reaction $^{18}O(p,\alpha)^{15}N$ around the resonance at 151 keV. The normalization consisted in dividing the excitation curve for the $^{18}O_2$-annealed sample by 380. (b) Excitation curves of the nuclear reaction $^{29}Si(p,\gamma)^{30}P$ around the resonance at 414 keV. The inset shows the region of the excitation curves corresponding to the surface. Symbols are the same as in Fig. 1.

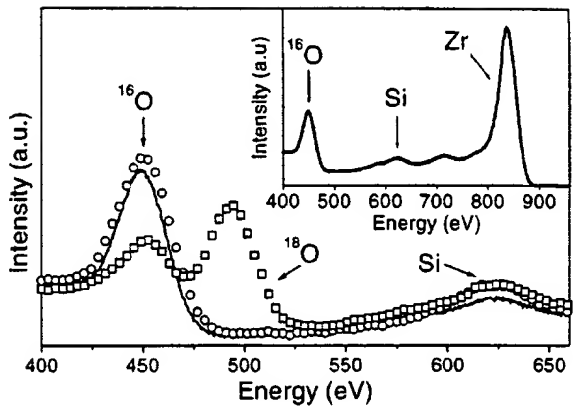

FIG. 3. Si and O signals in low energy ion scattering (ISS) spectra of 1000 eV He^+ ions. The complete spectrum for the as-deposited sample is shown in the inset. Symbols are the same as in Fig. 1.

and Si were determined by RBS in a channeling geometry:[10] 1 MeV He^+ ions were channeled in the ⟨001⟩ axis of the underlying Si(001) substrate and the scattered ions were detected in the grazing angle of 100° with respect to the direction of incidence. Figure 1(b) shows the channeled-RBS geometry and ^{16}O, ^{18}O, and Si signals in the spectra for as-deposited and annealed samples. The determined areal densities (in units of 10^{15}) for the as-deposited sample were 19.1 Zr/cm^2, 13.7 Si/cm^2, and 47.5 O/cm^2. After vacuum annealing, the areal densities of ^{16}O and Si remain constant within the accuracy of the measurement (5%). After $^{18}O_2$ annealing, Si areal density remains constant while ^{16}O and ^{18}O areal densities—8.5^{16}O/cm^2 and 37.6^{18}O/cm^2—reveal avery pronounced ^{16}O–^{18}O exchange, although the total amount of O in the silicate film remained essentially constant.

O and Si were profiled with subnanometric depth resolution using narrow, isolated nuclear resonance profiling (NRP),[11] with the $^{18}O(p,\alpha)^{15}N$ at 151 keV ($\Gamma_R = 100$ eV) and $^{29}Si(p,\gamma)^{30}P$ at 414 keV ($\Gamma_R \leq 100$ eV) nuclear resonances, respectively, with 60° sample tilt.[11,12] Normalized excitation curves for ^{18}O are shown in Fig. 2(a) and excitation curves for ^{29}Si in Fig. 2(b). These excitation curves can be converted into profiles using the program SPACES.[13] Both vacuum- and $^{18}O_2$-annealed samples present a concentration of Si in near-surface regions higher than the average values in the bulk of $ZrSi_xO_y$ films. This is seen in Fig. 2(b) recalling that sensitivity to Si in NRP is almost two orders of magnitude higher than in RBS. Surface selective, far more sensitive detection of Si is accomplished with low energy ion scattering (ISS) of 1000 eV He^+ ions[14] as shown in Fig. 3, confirming that the annealed samples have higher surface concentration of Si. The origin of this excess Si at the surface could be migration from the substrate across the oxide film as reported before for other high-K oxides deposited on Si.[15–17] This transport of Si from the substrate was so far unsuspected in $ZrSi_xO_y$ films and the present results are not sufficient to assure it. Since this may be deleterious to metal gate electrode/silicate interfaces due to silicide formation, it is imperative to understand the chemical environment of Si and of the other elements in the near-surface (and also near-interface) regions of the films, which is achieved here by angle-resolved x-ray photoelectron spectroscopy (ARXPS).

Zr 3d, O 1s, and Si 2p photoelectrons produced by Mg $K\alpha$ x rays were analyzed at different takeoff angles (Θ) between the normal to the sample surface and the axis of the energy analyzer.[17] This allows a comparison of the relative intensity ratios of all species present in near-surface (surface-sensitive mode, $\Theta = 60°$) and near-interface (bulk-sensitive mode, $\Theta = 25°$) regions as well as at intermediate values of Θ. Zr 3d photoelectron spectra obtained here for the as-deposited sample were identical to those already described in the literature[4] corresponding to the formation of Zr–O bonding in the vicinity of Si (Zr silicate) with no evidence of Zr–Si bonding. Results obtained after vacuum- and $^{18}O_2$-annealing at different takeoff angles did not provide any evidence of modification of the Zr chemical environment.

Figure 4 shows the O 1s region in surface- and bulk-sensitive modes. The spectra have been fitted with two components, which are related to O–Si and O–Zr bonds, as expected for Zr silicate.[4] The bulk-sensitive mode presents little change in relative intensities of the components for as-deposited and annealed samples, indicating chemical stability in the near-interface regions. On the other hand, the surface-sensitive mode displays an enhancement of the O–Si component in the $^{18}O_2$-annealed sample, while in the vacuum-annealed sample there is a decrease of this component, both cases are with respect to the as-deposited sample. This implies modifications of the chemical environment of O in the near-surface region depending on the kind of thermal annealing.

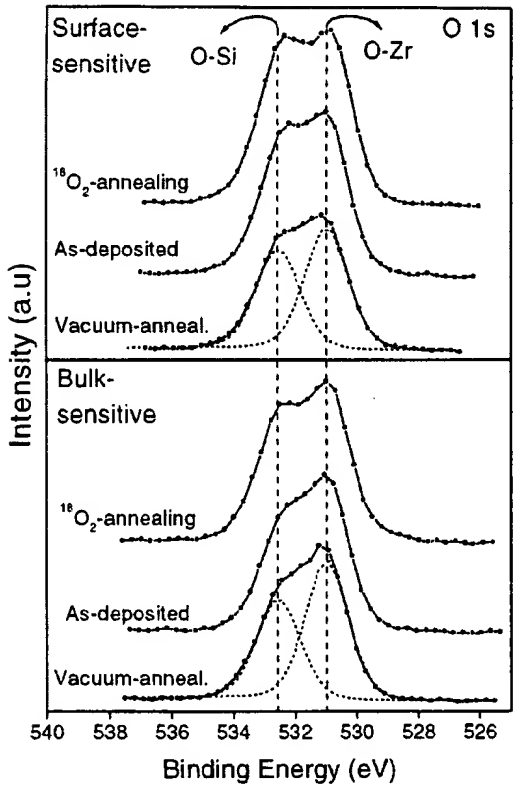

FIG. 4. O 1*s* region in surface sensitive ($\Theta = 60°$) and bulk-sensitive ($\Theta = 25°$) modes of ARXPS.

Figure 5 shows Si 2*p* ARXPS. The fitting procedure reveals Si–O–Zr bond[4] (Zr silicate environment of Si) and Si–O bond (Si oxide environment in silicate network), with a marked predominance of the Si–O–Zr component. In bulk-sensitive mode, the chemical situation of Si is not significantly affected by thermal annealing. However, the surface-sensitive mode reveals a Si–Si bond (Si in a Si environment) in the vacuum annealed sample, whereas the $^{18}O_2$-annealed sample remains essentially unchanged with respect to the as-deposited sample.

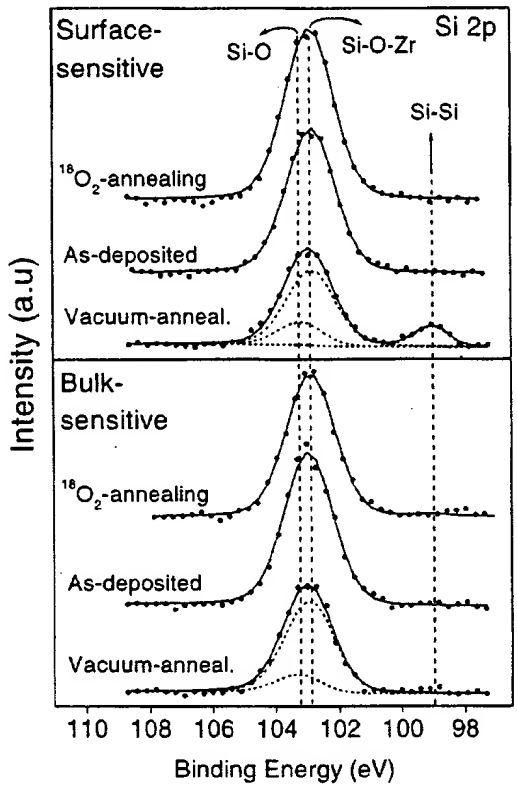

FIG. 5. Si 2*p* region in surface sensitive ($\Theta = 60°$) and bulk-sensitive ($\Theta = 25°$) modes of ARXPS.

Information provided by O 1*s* and Si 2*p* XPS analysis lead to attribution of different chemical status to Si atoms that migrate and accumulate in near-surface regions after vacuum and O_2 annealing, as observed by NRP and ISS. They apparently form Si precipitates under vacuum annealing, whereas under O_2 annealing, due to the abundant offer of O, the Si precipitates are either fully or partly oxidized with the remaining been reintegrated in the Zr silicate network (with different Zr, Si, and O proportions).

In summary, this work reports experimental evidence that the interface between deposited $ZrSi_xO_y$ films and the *c*-Si substrate remains stable, concerning atomic transport and chemical reaction, when submitted to thermal annealings at 600 °C in vacuum and in $^{18}O_2$ atmosphere. A strong ^{16}O–^{18}O exchange takes place throughout the whole silicate film during $^{18}O_2$ annealing, although without changing significantly the total amount of O in the films. On the other hand, the surface of the $ZrSi_xO_y$ films is not stable, presenting Si migration and accumulation. In the case of vacuum annealing, the accumulated Si atoms segregate in the form of silicon precipitates. This instability may have significant deleterious consequences once a metal electrode is deposited on the Zr silicate films, either before or after vacuum annealing, since metal silicides and silicates may be formed at the electrode/dielectric interface.

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Gadolinium silicate gate dielectric films with sub-1.5 nm equivalent oxide thickness

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$GdSi_xO_y$ gate dielectric films were deposited on Si(001) substrates using ultra-high-vacuum electron-beam evaporation from pressed-powder targets. Transmission electron microscopy showed that the films were amorphous as deposited and remained amorphous when annealed to temperatures up to 900 °C. Capacitance–voltage measurements indicate an equivalent oxide thickness (EOT) of 13.4 Å for a film with composition $GdSi_{0.56}O_{2.59}$ determined by *in situ* x-ray photoelectron emission spectroscopy. After forming gas annealing at 500 °C the EOT was reduced to 11.0 Å, at a physical thickness of 45 Å. The same film has a low leakage current of approximately 5.7×10^{-3} A cm^{-2} at +1 V, a reduction of 8.7×10^{4} compared to current density estimates of SiO_2 films with the same specific capacitance. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1356725]

The latest semiconductor roadmap described the replacement of the SiO_2 complementary metal–oxide–semiconductor (MOS) gate dielectric material as a "grand challenge" to Moore's law.[1] The requirement of 1–1.5 nm equivalent oxide thickness (EOT) by the 100 nm node has stimulated considerable research into alternate dielectrics, including Gd_2O_3,[2] Y_2O_3,[2,3] La_2O_3,[3,4] and silicates of Hf, Zr,[5–8] and yttrium.[9] An important consideration in the selection of materials is the compatibility with silicon.[10] To prevent the interfacial reactions observed for several of the pure oxides, Wilk and co-workers introduced the approach of using silicates.[5–7] This has the advantage of producing amorphous layers with good thermal stability, at the expense of a reduced dielectric constant (κ).

In this letter, we describe the properties of $GdSi_xO_y$ films deposited directly on Si(001). The substrates were 0.02–0.05 Ω cm *n*-type wafers, RCA HF last cleaned prior to deposition. Silicate films were deposited by electron-beam evaporation from a mixed, $(SiO_2)_{0.16}(Gd_2O_3)_{0.84}$ pressed-powder target in one chamber of a multichamber ultra-high-vacuum (UHV) system. Following deposition, the films were transferred *in vacuo* to a second UHV chamber and annealed *in situ* for 5 min at 800 °C. Au contacts of area 6.2×10^{-4} cm^2 were deposited onto the oxide films through a shadow mask in a third UHV chamber.

Figure 1 shows the *in situ* Gd 4*d* x-ray photoelectron spectroscopy (XPS) spectrum for an as-deposited $GdSi_xO_y$ film on Si, and the same film after UHV annealing.[11] The spectra were obtained at 23.5 eV pass energy and 45° photoelectron takeoff angle using unmonochromatized Mg $K\alpha$ photons (1254 eV) in a PHI 5000C system, integrated into the multichamber apparatus. The main features of the Gd 4*d* photoemission arise from multiplet splitting of the 4*d* hole with the $4f^7$ valence electrons to form ^9D and ^7D final ionic states.[12,13] The same spectral region also contains contributions from Si 2*s* peaks, related to the substrate and the silicate film. The separation and relative intensities of the Si 2*s* peaks were obtained from the Si 2*p* spectra, shown in Fig. 3.

The silicate O 1*s* spectrum is shown in Fig. 2. The intensity of the larger, higher-binding-energy film peak is not significantly changed by the anneal, but the full width at half maximum (FWHM) decreases from 2.3 to 1.8 eV. This suggests that the UHV annealing significantly reduces bond-length and bond-angle variations in the amorphous film. In comparison, the O 1*s* peak FWHM for a 170 Å thermal SiO_2 film analyzed using the same XPS instrument settings was 1.7 eV. The smaller peak at lower binding energy is due to hydroxide species, possibly $Gd(OH)_3$. Upon annealing, the peak intensity increases ~25%, which may result from residual water vapor in the UHV annealing chamber.

The Si 2*p* spectrum for the as-deposited film consists of

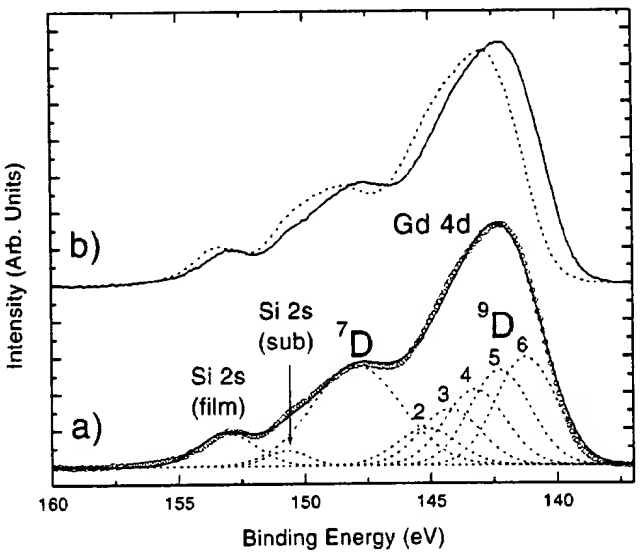

FIG. 1. (a) Gd 4*d* XPS spectrum after Shirley background subtraction (circles). The solid line is the convolution of the ^9D, ^7D, and Si 2*s* peaks (dashed lines). Relative to the main $\bar{J}=6$ peak, the relative intensities (positions) of the ^9D peaks are 0.88 (+1.02 eV), 0.70 (+2.01 eV), 0.52 (+3.00 eV), and 0.34 (+3.92 eV), for $\bar{J}=5$, 4, 3, and 2, respectively. (b) Comparison between the spectra obtained before (solid) and after (dashed) UHV annealing.

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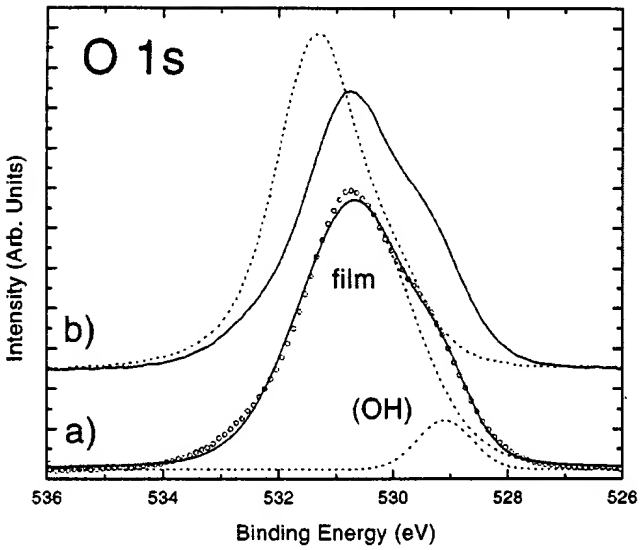

FIG. 2. (a) O 1*s* XPS spectrum after Shirley background subtraction (circles). The solid line is the convolution of the film peak and the peak due to hydroxide species (dashed lines). (b) Comparison between the spectra obtained before (solid) and after (dashed) UHV annealing.

two main peaks, related to the substrate and the silicate film (Fig. 3).[14] After UHV annealing, the film peak shifts to slightly higher binding energy, and increases slightly in intensity. The increase in the Si 2*p* film peak also suggests that the film oxidized slightly during the anneal due to residual water vapor in the annealing chamber. The O 1*s*:Si $2p_{3/2}$ (film) spacing increased from 429.0 to 429.2 eV after annealing but remained significantly smaller than the 429.6 eV spacing measured in SiO_2.[15]

From the integrated XPS intensities, the film composition was found to be $GdSi_{0.47}O_{2.48}$ before UHV annealing and $GdSi_{0.56}O_{2.59}$ afterwards. These values are similar to the stoichiometry of $Gd_2(SiO_4)O$ oxyorthosilicate, consisting of equal parts Gd_2O_3 and SiO_2.[16] The difference of 0.4 eV in the O 1*s*:Si $2p_{3/2}$ (film) spacing compared with the spacing

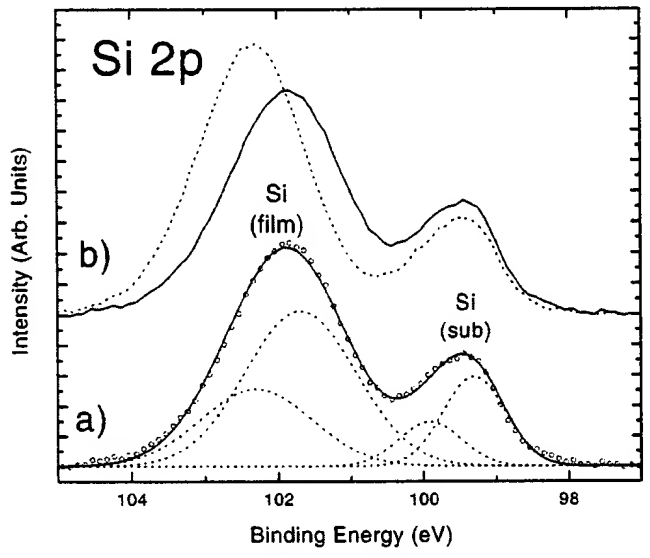

FIG. 3. (a) Si 2*p* XPS spectrum after Shirley background subtraction (circles). The solid line is the convolution of the substrate and film peaks, each having $2p_{3/2}$ and $2p_{1/2}$ components (dashed lines) in the ratio 2:1, with spin-orbit splitting 0.612 eV (Ref. 14). (b) Comparison between the spectra obtained before (solid) and after (dashed) UHV annealing.

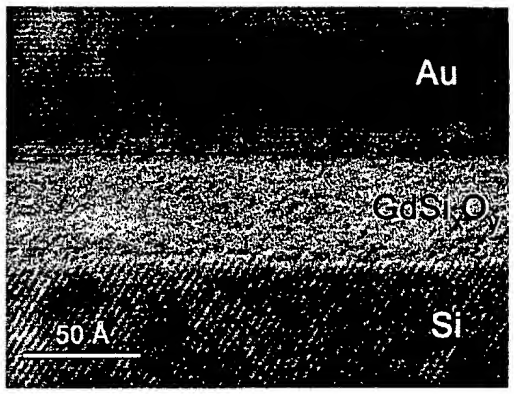

FIG. 4. TEM micrograph of Au/$GdSi_xO_y$/Si(001) capacitor after UHV annealing and PMA. The measurement was made on a Philips EM 430T operating at 250 keV.

in SiO_2 can be attributed to next-nearest effects of the Gd atoms bonded to oxygen atoms in the orthosilicate tetrahedra. In the (SiO_4) tetrahedra, the mean Si–O bond length is 1.63 Å, compared with 1.61 Å in SiO_2. Consistent with their highly electropositive character, the Gd atoms donate electronic charge to the Si–O bonds, and this results in the reduced O 1*s*:Si 2*p* spacing. The Si $2p_{3/2}$ (substrate):Si $2p_{3/2}$ (film) spacing increases from 2.4 to 2.9 eV after the UHV anneal. The smaller values, as compared to the value of 3.0 eV for SiO_2,[15] are consistent with this picture; however, charging and band-bending effects shift these peaks by different amounts making this spacing a less reliable measure of Si–O bonding.[15] Also consistent with this picture is the O 1*s*:Gd 4*d* ($^9D_6$) spacing of 389.4 eV, which is 0.7 eV greater than the spacing measured for a 250-Å-thick Gd_2O_3 film. This spacing is essentially unchanged by the UHV annealing, showing that the Gd–O bonds are not significantly affected by the anneal while the Si–O bonds are rearranged to some extent.

Films appear amorphous in transmission electron microscopy (TEM) micrographs (Fig. 4) and crystallization was not observed after annealing in UHV for 5 min at 800 °C or flowing N_2 for 2 min at 900 °C. We note that there is no evidence for the type of interfacial layer formation observed in our Gd_2O_3 films deposited directly on Si.[13,17]

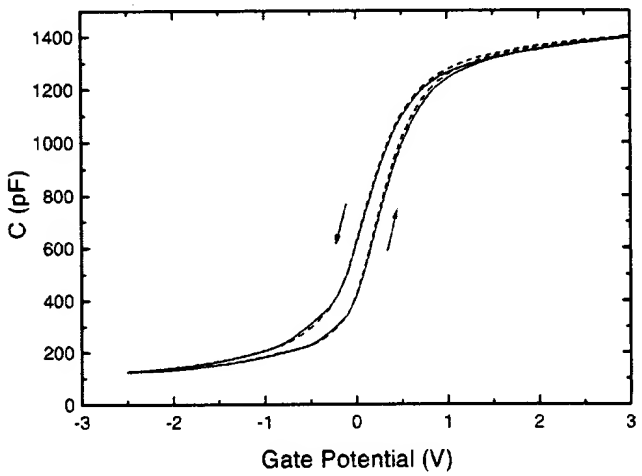

FIG. 5. Capacitance–voltage characteristics of the sample of Figs. 1–3 measured at 100 kHz (solid line) and 400 kHz (dashed line) at a step rate of 0.1 V s^{-1}.

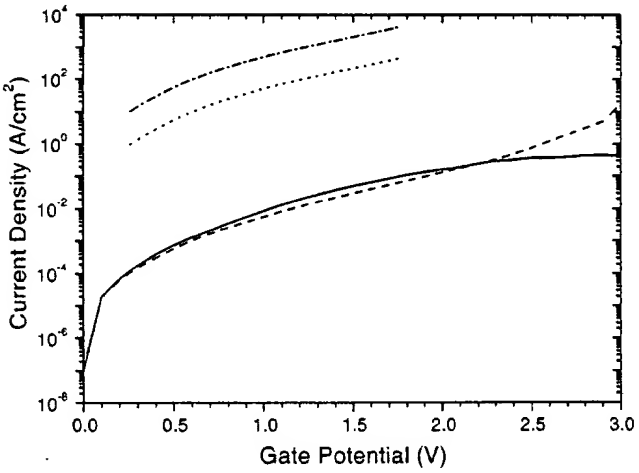

FIG. 6. Current density vs gate potential before (solid line) and after PMA (dashed line), stepped at 0.1 V s^{-1} from $-ve$ to $+ve$ and back to $-ve$. Calculated curves for SiO_2 films of thicknesses 13.4 Å (dotted line) and 11.0 Å (dot-dashed line) are shown for comparison.

Figure 5 shows the high-frequency capacitance–voltage (CV) characteristics. A counterclockwise hysteresis of 150 mV, indicative of charge trapping, is evident. The accumulation capacitance, corrected for quantum effects,[18] was used to calculate the EOT. For the film of Figs. 1–3 the result was 13.4 Å. The same UHV-annealed film was then given a 5 min postmetallization anneal (PMA) in forming gas (4% H_2 in N_2) at 500 °C. The measured EOT of 11.0 Å and the thickness of 45 Å (Fig. 4) indicate a dielectric constant of 15.8, assuming $\kappa = 3.85$ for SiO_2. After the PMA the hysteresis decreased slightly to 140 mV; however, the flatband voltage changed from 0.15 to −0.47 V, and the dispersion between 100 and 400 kHz increased dramatically for negative potentials, indicating an increased density of interface states in the lower half of the band gap. Using a work function for Au of 5.0 eV, rather large positive effective trapped interface charge densities of 1.3×10^{13} and 2.5×10^{13} cm^{-2}, respectively, are calculated from the measured flatband voltages before and after the PMA. It was suggested that similar positive charges in La_2O_3 films resulted from oxygen vacancies or $(OH)^-$ ions occupying O_2^{2-} sites.[3] This hypothesis is consistent with our XPS O 1s peak analysis, indicating a measurable quantity of hydroxide species in our films, which may diffuse into the films during the PMA.

As shown in Fig. 6, the PMA reduced the current density slightly at lower potentials but increased the current at gate potentials above 2.2 V. This increase and the deterioration in CV characteristics after the PMA were also evident for N_2 anneals and may be associated with an interaction between the gold and the Gd silicate. Figure 6 also shows the current density for 13.4- and 11.0-Å-thick SiO_2 films extrapolated from the data of Brar, Wilk, and Seabaugh for n-type Si(001) and Al gates.[19] The measured current densities at 1 V were 8.7×10^{-3} and 5.7×10^{-3} A cm^{-2} for the samples before and after the PMA, representing current reductions of 5.9×10^3 and 8.7×10^4 relative to the calculated values for SiO_2.

In summary, these $GdSi_xO_y$ films exhibit favorable properties for use as a replacement MOS gate insulator, including moderate dielectric constant and resistance to crystallization at temperatures up to 900 °C. The current density reduction over SiO_2 with an EOT of 11.0 Å is 8.7×10^4 at 1 V. However, integration of this material into device processing will require the use of an alternative technique to electron-beam deposition to reduce possible interface damage. The material quality can also be improved by reducing the incorporation of hydroxide species upon UHV and postmetallization annealing.

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Structure and stability of La_2O_3/SiO_2 layers on Si(001)

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High-resolution transmission electron microscopy and electron energy-loss spectroscopy (EELS) were used to investigate $La_2O_3/SiO_2/Si$ structures. The La_2O_3 layers were deposited on thermal SiO_2 on silicon, followed by rapid thermal annealing treatments at 600 °C and 800 °C in a nitrogen ambient. After annealing at 600 °C, the oxide layers were amorphous. After an 800 °C treatment, crystallites appeared in the original La_2O_3 layer, and the total oxide layer thickness increased by 17%, most likely due to the oxygen diffusion and reaction at the Si/SiO_2 interface. EELS, using a 0.2 nm probe, showed that rapid thermal annealing at 600 °C did not cause significant La diffusion into the SiO_2 layer, whereas some intermixing was observed at 800 °C. We use the observed microstructures to estimate equivalent oxide thicknesses. The results demonstrate that oxygen partial pressures and initial SiO_2 thickness need to be carefully controlled to control SiO_2 formation at the Si interface and to achieve target equivalent oxide thickness. © *2001 American Institute of Physics.* [DOI: 10.1063/1.1383268]

Technology roadmaps predict that continued scaling of complementary metal–oxide–semiconductor devices would eventually require a gate dielectric with a capacitance equivalent to that of SiO_2 of less than 1.5 nm thickness, a thickness regime where tunneling currents through SiO_2 become unacceptably high for many applications.[1] Replacing SiO_2 with a material with a higher dielectric constant (k) would allow physically thicker films to achieve the required capacitance values. Two important issues are the thermal stability of the alternative gate dielectric on silicon and the electrical quality of the interface.

Metal oxides, which are potentially thermally stable in contact with silicon, include Al_2O_3, La_2O_3, ZrO_2, and HfO_2.[2] However, the excellent electrical properties of the Si/SiO_2 gate dielectric stacks may not be achieved for the Si/high-k heterostructures.[3] Large flat band voltage shifts are often reported for gate dielectric stacks using alternative oxides, for reasons that are presently not well understood.[4] Depositing metal oxides on oxidized silicon and the subsequent reaction to a silicate could potentially preserve some of the properties of a high-quality SiO_2/Si interface. For La_2O_3 and Y_2O_3 films on Si and SiO_2, silicate formation has been reported during annealing treatments,[5,6] although the bulk solid-state reactions are known to be sluggish.[7,8] ZrO_2 has been reported not to react with SiO_2.[9] Oxygen diffusion through the metal oxide might cause the growth of SiO_2 at the Si interface,[5,10] reducing the overall capacitance values. The metal oxide might crystallize before the reaction to the silicate is completed. Here, we report results of investigations of the reaction behavior of a La_2O_3/SiO_2 gate dielectric stack subjected to rapid thermal anneals at two different temperatures by high-resolution imaging and electron energy-loss spectroscopy (EELS) in a transmission electron microscope.

La_2O_3 films were deposited on a standard thermal oxide of about 2 nm thickness on a uniformly doped ($10^{18}/cm^3$ boron) p-type silicon wafer. Lanthanum was reactively evaporated from a high-temperature effusion cell in an oxide molecular beam epitaxy system in the presence of molecular oxygen. The substrate temperature during deposition was 300 °C. The chamber pressure during deposition was 1.5×10^{-5} Torr. Metal fluxes were about 10^{15}atoms/cm^2 s. The thickness of the La_2O_3 film was about 2.3 nm. Postdeposition high-temperature anneals were performed for 30 s in a rapid thermal annealing furnace in reagent grade nitrogen. Annealing temperatures were 600 °C and 800 °C, respectively. Capacitor structures were fabricated by magnetron sputtering of Pt electrodes. The electric and dielectric properties of these gate dielectric stacks will be reported elsewhere.

Samples for transmission electron microscopy (TEM) were prepared by standard cross section techniques with argon ion milling as the final step. The film microstructure and chemistry were investigated using a 200 kV transmission electron microscope (JEOL JEM 2010F) equipped with a field-emission gun, an annular dark-field (ADF) detector, and a postcolumn imaging filter (Gatan GIF200). This microscope is capable of achieving of sub-0.2 nm probe sizes for microanalysis and incoherent Z-contrast lattice imaging.[11] Images and spectra were recorded from regions that were covered by the Pt top electrode, as preliminary studies indicated ion-milling damage in uncovered regions. For EELS, the microscope was operated in scanning transmission electron microscopy (STEM) mode. In STEM, a lattice resolution Z-contrast image was acquired on the ADF detector surrounding the imaging filter. Resolution of the Si lattice

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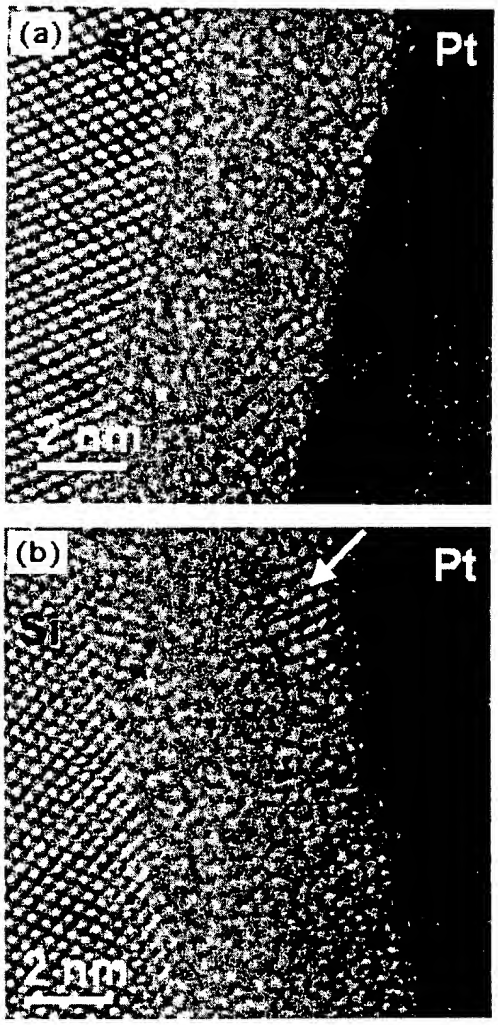

FIG. 1. Cross section HRTEM micrographs of (a) the sample annealed at 600 °C and (b) the sample annealed at 800 °C are shown.

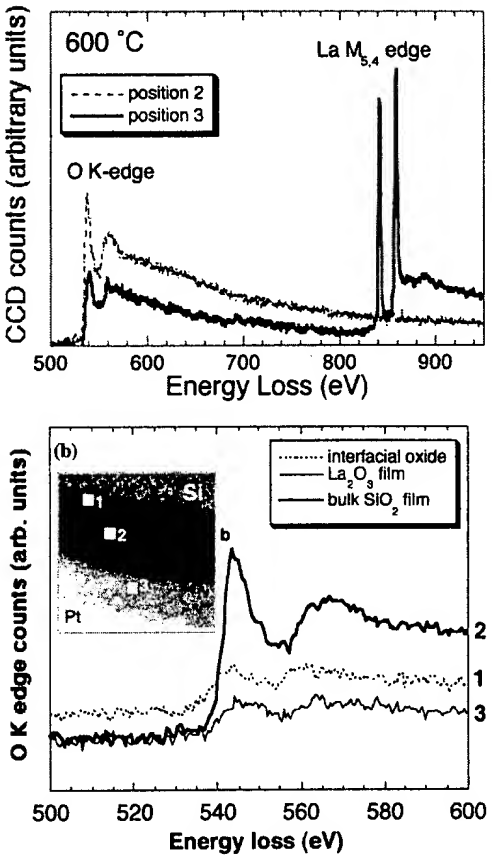

FIG. 2. (a) Oxygen *K* edges and La *M* edges recorded from the oxide layers that exhibited different contrasts in Fig. 1(a) (600 °C sample) are shown. The location of the probe (denoted "2" and "3," respectively) is indicated in the inset in (b), an atomic resolution *Z*-contrast image. Note the atomic number sensitivity of the *Z*-contrast image. (b) Fine structure of the oxygen *K* edges recorded from the different positions shown in the inset. Note the decrease in the first bulk peak denoted "*b*," reflecting the substoichiometry as well as the reduced edge onset of the interfacial SiO_2.

planes confirmed a probe size of no more than 0.27 nm; more importantly, the *Z*-contrast image was used to position the probe at different positions within the layers. The EELS spectrum could be acquired immediately without changing the optical parameters of the microscope. Oxygen *K* edges as well as La *M* edges were recorded from different positions within the oxide layers. The Si *L* edge and the La *N* edge appear at the same energy loss (99 eV); therefore, only indirect information on the diffusion of Si from the SiO_2 into the La_2O_3 layer could be obtained.

Figure 1 shows conventional cross sectional high-resolution TEM (HRTEM) images recorded along ⟨110⟩ Si of the samples annealed at 600 °C [Fig. 1(a)] and 800 °C [Fig. 1(b)], respectively. The amorphous oxide appears to consist of two layers exhibiting different image contrast. The darker layer is adjacent to the Pt electrode. The oxide layer annealed at 600 °C is fully amorphous. In the 800 °C sample, small crystallites appear in the darker layer [see arrow in Fig. 1(b)]. The total thickness of the oxide layer increased by about 17%, from about 4.3 nm ± 0.2 nm (600 °C sample) to 4.9 nm ± 0.24 nm due to annealing at higher temperatures (800 °C sample). The "two-layer" image contrast could be due to the diffusion of the Pt electrode into the layers, as proposed for Al electrodes and silicate layers.[12] or due to chemically distinct SiO_2- and La_2O_3-like layers.

Figure 2(a) shows O *K* edges and La *M* edges recorded from the interior of the layers exhibiting bright and dark contrast in HRTEM of the 600 °C sample. The probe positions are marked in the atomic resolution ADF image [inset in Fig. 2(b)]. No La can be detected in the layer with brighter contrast in HRTEM (dark layer in the ADF image) within the detection limit of the method. In contrast, the layer adjacent to the Pt electrode is La rich, and shows less intensity in the oxygen *K* edge. Figure 2(b) shows a comparison of the fine structures of an oxygen *K* edge recorded from the Si/SiO_2 interface, from the interior of the SiO_2 layer and from the La_2O_3 layer. The interfacial SiO_2 shows a reduced intensity in the peak denoted "*b*," and a reduced edge onset that can be interpreted as induced band gap states.[13] Rapid thermal annealing at 600 °C was insufficient to cause diffusion of La into the SiO_2 layer; the contrast in the image arises from the presence of two chemically distinct layers, SiO_2 and La_2O_3.

Figure 3 shows typical EELS spectra recorded from three different positions within the oxide layers of the sample annealed at 800 °C (the approximate distance from the Si interface is indicated in Fig. 3). The layers with different contrasts in HRTEM and ADF show a pronounced difference in chemistry. Some La can be detected in the bright layer, as

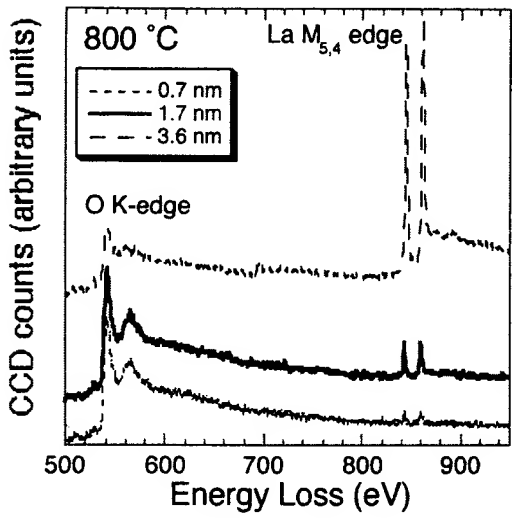

FIG. 3. Oxygen K edges and La M edges recorded from the interior of the oxide layers of the 800 °C sample are shown. The approximate distance (±0.2 nm) from the Si interface is indicated for each spectrum.

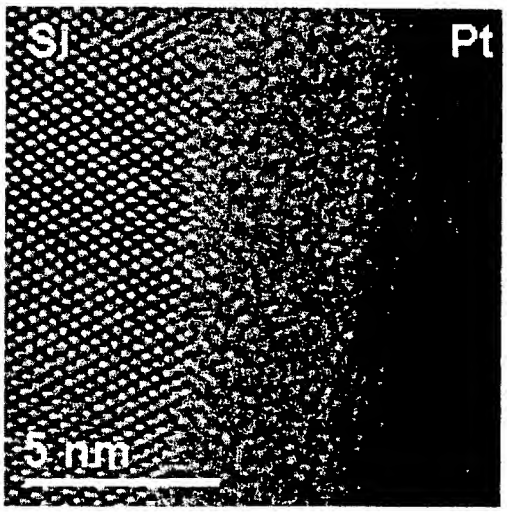

FIG. 4. Cross section HRTEM micrograph of a La_2O_3 film deposited on a chemical SiO_2 is shown. The total oxide thickness is about 4.4 nm.

can be seen from the appearance of La M edges in the spectrum taken from this region ("1.7 nm"), with less La close to the Si interface ("0.7 nm"). Therefore, annealing at 800 °C causes some rearrangement of atoms, as exhibited by the crystallization of the original La_2O_3 layer and some diffusion of La into SiO_2.

In summary, the strong contrast differences of the two layers in HRTEM and ADF, the absence of La in the SiO_2 layer adjacent to the Si, show that no single-phase, homogenous lanthanum silicate is formed during the annealing experiments. This is probably due to a relatively sluggish reaction and the formation of new SiO_2 at the Si/SiO_2 by oxygen diffusion through the oxide layers during annealing. Reagent nitrogen contains approximately 1 ppm O_2, corresponding to an O_2 partial pressure of $\sim 1\times 10^{-3}$ Torr. The observed thickness increase (Fig. 1) can be explained with the formation of SiO_2 at the Si/SiO_2 interface during the 800 °C treatment. Though no information on Si in the La_2O_3 layer could be obtained by EELS, crystallization in the 800 °C treated sample indicates that the uppermost oxide layer contains less than 40% SiO_2.[14] The observed microstructures can be used to conservatively estimate the equivalent oxide thicknesses, EOT. The equivalent oxide thickness is estimated as

$$\mathrm{EOT} = t_{\mathrm{dielectric}} \times (\epsilon_{SiO_2}/\epsilon_{\mathrm{dielectric}}),$$

with $t_{\mathrm{dielectric}}$ corresponding to the total physical thickness of the gate dielectric stack and $\epsilon_{\mathrm{dielectric}}$ the dielectric constant calculated from the measured thicknesses and theoretical values for the dielectric constants ($\epsilon_{SiO_2}=3.9$, $\epsilon_{La_2O_3}=25$). For the 600 °C sample, we estimate an EOT of 2.5 nm. For the 800 °C sample, we can give an upper limit of an EOT of 2.8 nm (with a silicate interlayer of $\epsilon_{La_2O_3,SiO_2}=17$, assuming no reduction in the dielectric constant of the upper La_2O_3 layer due to Si diffusion). Future work should include annealing conditions that control temperature and the oxygen partial pressure over a range of values, as the oxygen diffusivities of rare-earth oxides are very high,[15] and optimization of the initial SiO_2 thickness. Initial results are shown in Fig. 4, a HRTEM image of a La_2O_3 thin film deposited on a thinner (8–12 Å) chemical SiO_2 after rapid thermal annealing at 1000 °C. No crystallization can be detected, and an EOT of 1.8 nm is estimated for this oxide stack, consistent with dielectric measurements.[16]

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